



ABSTRACT

This manual describes Ball Computer Product's Nova-line controller for phase encoded magnetic tape drives and outlines its specifications, operation and installation.

Date: 12/73

Pages: 30

3180 MAGNETIC TAPE CONTROLLER
TECHNICAL MANUAL
81-3460070-1

Copyright© 1973 By Ball Computer Products Division

The designs, information, and data contained herein is proprietary and is submitted in confidence, and shall not be disclosed, used, or duplicated, in whole or in part, for any purposes whatsoever without prior written permission of Ball Computer Products, 860 East Arques Avenue, Sunnyvale, California 94086. This legend shall be marked on any reproduction hereof in whole or in part. Receipt of this document shall be deemed to be an acceptance of the conditions specified herein.

ADDENDUM
3180 TAPE CONTROLLER

The current design of the 3180 Controller incorporates low-power Schottky logic, reducing the power requirements to 5.0 volts at 4.5 amperes. The schematics, at the conclusion of this manual, reflect the current design level.

TABLE OF CONTENTS

	PAGE
SECTION I - GENERAL INFORMATION	
1.0 Scope	1-1
1.1 Introduction	1-1
1.2 Specifications	1-2
SECTION II - PROGRAMMING CONVENTIONS	
2.1 Scope	2-1
2.2 Phase Encoded Recording	2-1
2.3 Tape Organization	2-2
2.4 Programming	2-5
2.5 Nova Conventions	2-15
SECTION III - INSTALLATION	
3.1 Scope	3-1
3.2 Unpacking and Inspection	3-1
3.3 Repacking for Shipment	3-2
3.4 Slide Mounted Rack Preparation	3-2
3.5 Installation	3-3
3.6 Multiple Drive Interface	3-9
APPENDICES	
Appendix A - Wang Mod 10 and Mod 11 Interface	

SECTION I - GENERAL INFORMATION

1.1 Scope

This manual introduces the reader to the DECISION Model 3180 Magnetic Tape Controller. The first section describes the controller briefly and outlines its specifications. Section II describes its operation and programming conventions while Section III outlines the installation and interface procedures.

1.2 Introduction

The DECISION 3180 Magnetic Tape Controller interfaces any of the Data General Nova-series minicomputers with the unformatted type phase encoded (PE) magnetic tape drives. The controller can operate up to four drives simultaneously at any standard tape speed to 150 ips. Drives are nine-track, 1600 bpi density with the tape format and error-checking conventions compatible with IBM phase encoded standards. The controller incorporates all formatting functions required to operate phase encoded drives and the necessary interface to the Nova computer, serving as both a "formatter" and "adapter" in a single unit. Automatic de-skewing of up to four characters is provided with data recovery accomplished using a phase-locked-loop decoding technique. The controller incorporates two full 16-bit word buffers to significantly reduce the occurrence of data channel access problems characteristic of high-speed devices.

The controller is supplied as a single circuit card that can be inserted easily into one of the Nova's I/O sub-assembly slots and an adapter assembly designed to interface directly with the specified tape drive. Software available includes a rigorous diagnostic program and two device drivers; one for stand-alone operation and one to operate in conjunction with the DECISION Disk Operating System (DDOS).

1.3 Specifications

Specification for the 3180 Magnetic Tape Controller are listed in the following table (Table 1-1).

TABLE 1-1
SPECIFICATIONS

COMPATIBILITY	
CPU	Any Data General Nova-line minicomputer.
TAPE DRIVES	Unformatted phase encoded drives with dual gap heads. Manufacturers include, but are not limited to: Wangco, Pertec, Kennedy, Bright Industries. Up to four drives may be interfaced to a controller via a "daisy chain" technique provided all drives are from the same manufacturer and operate at the same tape speed.
TAPE FORMAT	
TAPE	Computer grade, 0.5 inch wide ANSI standard with reflective BOT and EOT markers.

TABLE 1-1 (cont.)

DENSITY	1600 characters per inch (cpi).
FORMAT	IBM compatible, 9 track.
DATA PACKAGING	Controller arranges 16-bit data word into two tape characters.
SPEED	12.5, 25, 37.5, 45, 75, 100, 112.5 or 150 inches per second (ips). Tape speed supported specified at time of manufacture (may be field altered).
PARITY	Odd parity. Vertical parity across a character written and verified on all drives. As a diagnostic aid, even parity may be selected.
PHYSICAL	
DIMENSIONS	15" x 15" x 1/2" (l x w x h)
WEIGHT	18 oz. (net) 8 lbs. (shipping)
POWER	5.0 volts ("±" 0.2V) at 7.8 Amps; supplied from Nova back plane.
ENVIRONMENTAL	Temperature 0-70°C Humidity 0-100% (non-condensing).
ACCESSORIES SUPPLIED	
HARDWARE	3180 Magnetic Tape Controller. Adapter board assembly. Two (2) 10-foot controller to adapter interface cables. 3180 Technical Manual.

TABLE 1-1 (cont.)

SOFTWARE*	3180 Exerciser tape and manual.
	3180 Diagnostic tape and manual.
	Magnetic Tape Drivers tape and manual.

- * Software supplied may vary with recipient. Write certain OEM agreements, software only supplied initially.

SECTION II - PROGRAMMING CONVENTIONS

2.1 Scope

This section describes the phase encoded recording technique, tape format and programming conventions for the 3180 Phase Encoded Tape Controller.

2.2 Phase Encoded Recording

With the phase encoded (PE) technique, information is recorded by altering the direction of flux transitions occurring at the center of a bit cell. 1600 of these cells are contained in a linear inch of tape or 1600 bits per inch. Referring to Figure 2-1, a flux transition towards the Inter Record Gap (IRG) flux direction is defined as a "1" while a flux transition away from the IRG flux direction is defined as a "0". To allow recording by this method of a succession of ones and zeros, flux transitions are made at the boundaries of the bit cell (if required) to establish the proper polarity for the center transition as shown for the bit sequence 0110001.

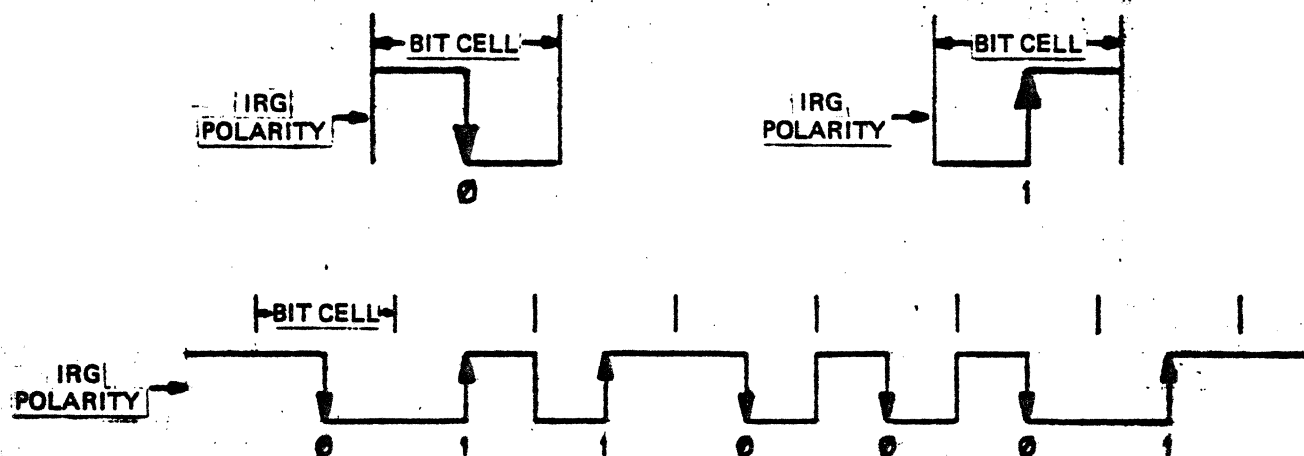


FIGURE 2-1

BIT CELL FLUX TRANSITIONS

2.3 Tape Organization

As with standard NRZI recording, PE recording groups data into records and files. Records are separated by 0.6 inch erased gaps (inter-record gaps) on the tape and groups of records may be partitioned into files through the use of file marks. Figure 2-2 depicts the PE data block and IRG format.

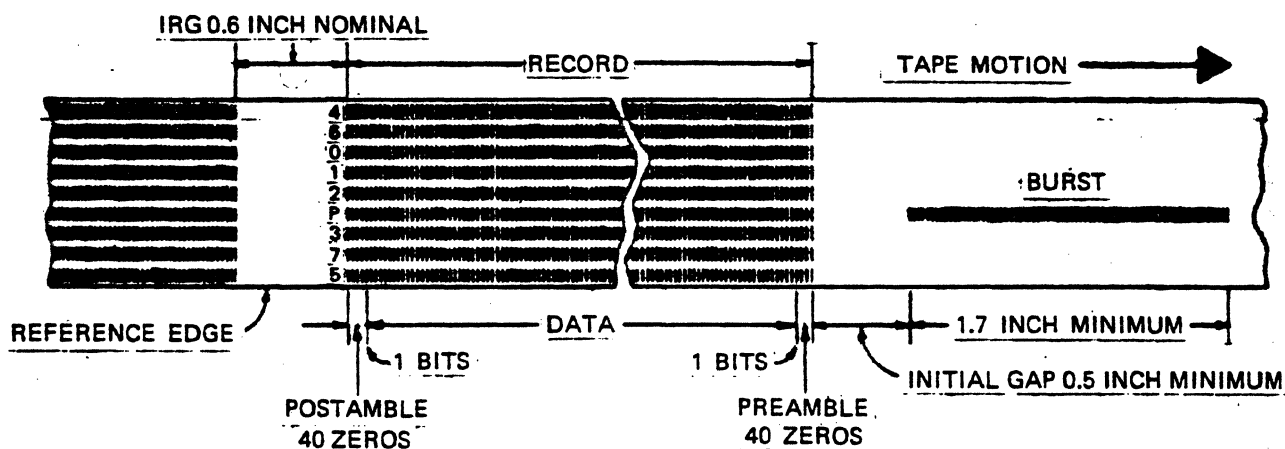


FIGURE 2-2

PE TAPE FORMAT

2.3.1 Identification Burst

A 1600 frpi (flux reversals per inch) identification burst is initially written on the tape when a write operation is initiated from the "Beginning Of Tape" (BOT) reflective marker. This burst identifies the tape as containing phase encoded data. The burst consists of a bit sequence at 1600 frpi in the parity (P) track, beginning 1.7 inches (minimum) before the trailing edge of the load point (BOT) marker and continuing past the marker. An initial gap of 0.5 inches (minimum) follows the identification burst.

2.3.2 Preamble

A preamble consisting of 41 characters precedes the data in every record. The first 40 characters are zeros followed by a single all "1"s character (a 1 bit in each of the nine tracks). The string of zero bits allows the controller's data recovery logic to synchronize

with the data read from tape while the single "1" bit indicates the start of data block.

2.3.3 Postamble

A postamble concludes every data record and consists of a single all "1"s bit followed by 40 zero bits.

2.3.4 Inter-Record Gap

An Inter-Record Gap (IRG) follows every record and consists of a 0.6 inch (nominal) erase gap.

2.3.5 End-of-File Mark

Groups of records may be separated into files by an End-of-File (EOF) mark. As shown in Figure 2-3, an EOF mark is written 3.5 inches from the last record within the file and consists of 80 flux reversal (40 bits) at 3200 frpi in tracks P,0,2,5,6 and 7 while channels 1,3 and 4 are erased in the direction of the IRG.

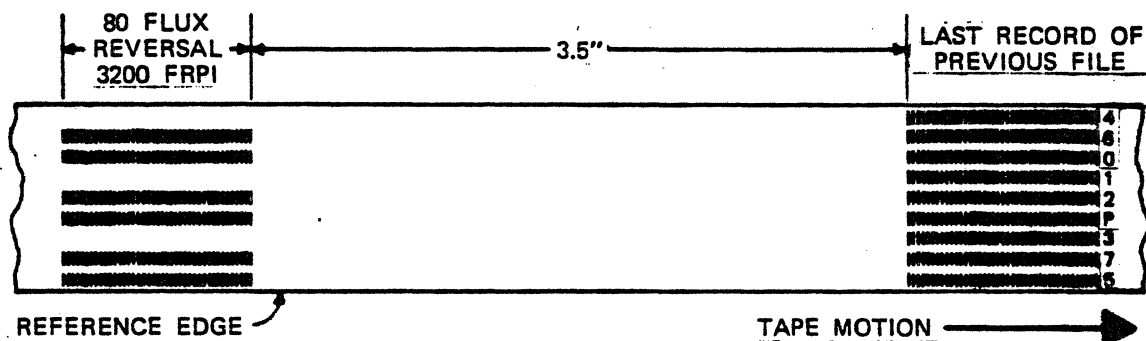


FIGURE 2-3

END-OF-FILE MARK

2.4 Programming

All controller operations are under program control. The controller uses the Nova's data (DMA) channel to transfer information. The programmer must specify the operation to be performed, a starting memory address location for the data transferred and the number of words to be transferred.

The controller follows the Data General conventions in the use of the Busy and Done flags and the data channel and interrupt logic.

The Nova I/O instruction words exhibit the following format.

I/O INSTRUCTION

0 1 1			AC ADDRESS		OPERATION			FUNCTION		DEVICE CODE					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bits 0,1 and 2 (011) define the instruction as an I/O operation.

Bits 3 and 4 select one of the Nova's four accumulators as the source or destination of the control or status word transferred. When an I/O instruction does not require an accumulator, the 3rd and 4th bits are ignored.

Bits 5,6 and 7 select the I/O operation to be performed.

Bits 8 and 9 select a function to be performed by the controller. A single instruction can specify both an operation and a function.

Bits 10 through 15 specify the octal device code. The 3180 controller normally responds to device code 22₈, identified by the mnemonic MTA. (A simple adjustment can arrange the controller to respond to device code 62₈).

2.4.1 I/O Operations

The I/O operation is determined by the states of bits 5,6 and 7 of the instruction word. The following operations transfer all control information to or from the controller.

Data Out A (DOA n,MTA)

The DOA instruction loads the contents of bits 8-15 from accumulator "n" (bits 3 and 4) into the controller's A (control) register.

A REGISTER

NOT USED								Thres- hold	Parity	OPERATION			NOT USED	DRIVE	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Threshold: The threshold bit (bit 8) selects the read threshold (clipping) level on drives with selectable threshold levels. If the threshold bit is zero, the normal threshold level is selected while if the bit is one, the low threshold level is selected.

Parity: The parity bit (bit 9) selects the vertical character parity and is normally set to zero, enforcing odd parity across the character.

Operation: Bits 10-12 select the command to be executed by the next (or concurrent) Start (S) command as follows:

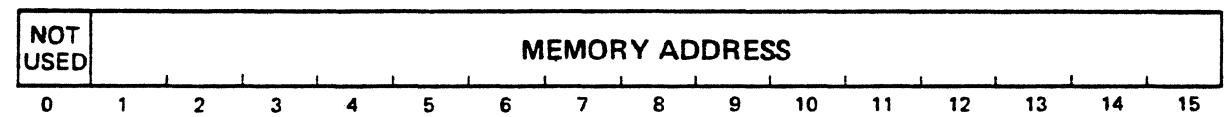
- 0 (000) - Read
- 1 (001) - Rewind
- 2 (010) - Off-line
- 3 (011) - Space Forward
- 4 (100) - Space Reverse
- 5 (101) - Write
- 6 (110) - Write End-of-File
- 7 (111) - Erase

Drive: Bits 14 and 15 specify the addressed drive (0-3).

Data Out B (DOB n,MTA)

The DOB instruction loads the contents of the selected accumulator (n) into the controller's B (memory address) register.

B REGISTER



Bits 1-15 of the accumulator word (bit 0 is ignored) specify the memory location of the first data word to be transferred.

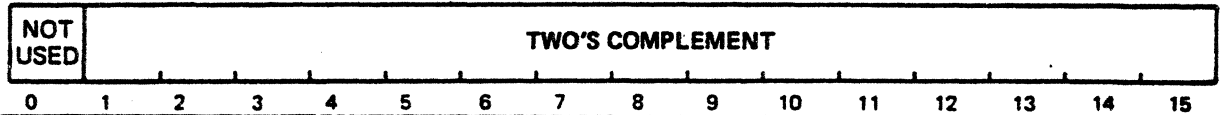
The B register is subsequently incremented each time a word is transferred.

Data Out C (DOC n,MTA)

The DOC instruction loads bits 1-15 (bit 0 is ignored) of the selected accumulator (n) into the controller's C (word count)

register. When the controller is in the read or write mode, the register is loaded with the two's complement of the number of words to be transferred while when in the space forward or space reverse mode, the register is loaded with the 2's complement of the number of records to be spaced over.

C REGISTER



Data In A (DIA n,MTA)

The DIA instruction loads the specified accumulator with the contents of controller's status register. The interpretation of the status register is as follows:

STATUS REGISTER

error	data late	re- winding	illegal	high density	parity error	end of tape	end of file	load point	nine track	bad tape	send clock	first char	write lock	odd char	ready
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit 0: ERROR. An error has occurred as indicated by the setting of bits 1,3,5,6,7,8,10 or 14.

Bit 1: DATA LATE. The data channel did not respond to the controller's request for access within the required time period. During a write operation, this error will immediately terminate the operation, causing the controller to set Done while during a read operation, the transfer will continue until either the end-of-record is reached or the the word count is satisfied.

Bit 2: REWINDING. The addressed dirve is currently rewinding.

Bit 3: ILLEGAL. This bit will be set if, when a start command is issued, any of the following conditions exist:

1. The operation specified is "Write", "Erase" or "Write EOF" and the tape reel is not write enabled (write protect ring missing).
2. The operation specified is "Space Reverse" and the tape is at its load point (BOT) marker.
3. Busy is not set and the addressed drive is not ready.

Setting "Illegal" prevents execution of further commands and causes the controller to set Done. Following an "Illegal" condition, a Clear (NIOC) command must be issued to clear the status register in order to allow operation to resume.

Bit 4: HIGH DENSITY. This bit is permanently set to zero.

Bit 5: PARITY ERROR. This bit is set when the controller encounters a character with the "incorrect" parity.

Bit 6: END OF TAPE. This bit is set when the tape reaches (or passes) the End-of-Tape (EOT) reflective marker.

Bit 7: END OF FILE. This bit is set whenever the controller writes, reads or spaces over an End-of-File (EOF) mark.

Bit 8: LOAD POINT. When set, this bit indicates that the tape is at the load point (BOT) marker.

Bit 9: NINE TRACK. This bit is always set indicating that the drive is a nine track drive.

Bit 10: BAD TAPE. This bit is set when the controller encounters a segment of tape containing excessive character skew or a dropout in one or more tracks. During a read operation the setting of this bit terminates the transfer,

sending the controller Done.

Bit 11: SEND CLOCK. A diagnostic bit.

Bit 12: FIRST CHARACTER. A diagnostic bit.

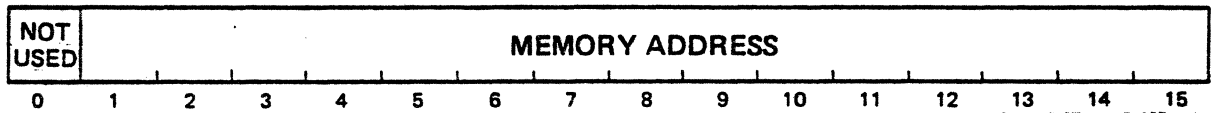
Bit 13: WRITE LOCK. When set, this bit indicates that the write enable ring is not in place on the source tape reel of the addressed drive.

Bit 14: ODD CHARACTER. The assertion of this bit indicates that the number of characters read in the record was odd.

Bit 15: READY. When set, this bit indicates that the addressed drive is idle and ready to accept a command.

Data In B (DIB n,MTA)

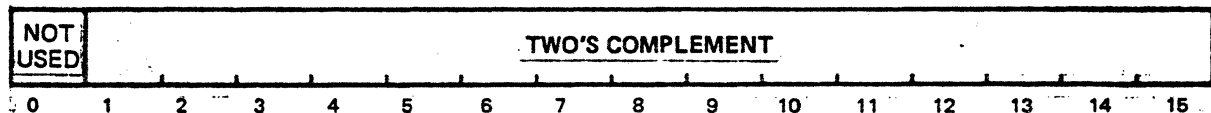
B REGISTER



The DIB instruction loads the specified accumulator with the contents of the controller's B (memory address) register with Bit 0 set to zero.

Data In C (DIC n,MTA)

C REGISTER



The DIC instruction loads the specified accumulator with the contents of the controller's C (word count) register. The C register word represents the two's complement of either the number of words to be transferred during a read or write operation or the number of records to be spaced over during a space forward or space reverse operation. When the DIC command is issued prior to the completion of the intended operation, bit 0 will be set to one.

2.4.2 I/O Functions

The function, as previously stated, is determined by the states of bits 8 and 9 of the instruction word. Any of the I/O operations can include a function or a function can be an independent command, without an associated operation (NIO) and without involving an accumulator. The I/O functions are implemented as follows:

F=00 (NIO)	No action. If combined with an associated I/O operation, perform the operation as indicated by bits 5, 6 and 7, but do not initiate command execution.
F=01 (NIOS)	Start (mnemonic S). If combined with an I/O operation, perform the associated operation and execute the command. Set Busy for the duration of command execution. When complete, clear Busy and set Done.
F=10 (NIOC)	Clear (mnemonic C). Stop any current operation. Clear Busy and Done and all registers.
F=11 (NIOP)	Pulse (mnemonic P). Not used.

2.4.3 Command Execution

When the controller receives an isolated (NIOS) or coupled (DOAS, etc.) START command, it will execute the command specified by bits 10, 11 and 12 of the A (control) register as described below.

READ (command 0₈)

The controller places the addressed drive into the read mode and starts the tape in the forward direction. The characters read are assembled into 16-bit words (2 characters per word) and transferred into the computer through the data channel. The core location of the first word transferred and the number of words to be transferred are determined by the contents of the B and C registers respectively.

The data transfer is terminated at the end of a record or when the number of words specified by the C register has been transferred. If the C register specifies fewer words than are contained in the record, the remainder of the record will not be read. If the record contains less words than specified by the C register, the transfer will terminate at the end of the record and the two's complement of the remaining number of words to be read will remain in the C register following the transfer. The controller will always stop the tape in an inter-record gap.

If the number of characters transferred is odd, the controller will place the odd character in bits 8-15, force bits 0-7 to zero and set S14 (Odd Character) while if a file mark is encountered during the read operation, the controller will immediately go Done, terminating the

the transfer and setting S7 (End-of-File). No data transfer will be initiated in the case of an end-of-file mark.

REWIND (command 1_g)

The controller rewinds the addressed drive. If no illegal condition exists (S3 set), the tape will rewind to the load point (BOT) marker or, if at the load point, will unload. If an illegal condition exists when the rewind command is issued, the controller will set S3 (Illegal) and subsequently go Done. The Rewind command itself will not set Busy or Done.

OFFLINE (command 2_g)

The controller places the addressed drive off-line, disabling the drive and all drive status lines. Once a drive has been placed off-line, it can only be placed on-line again from its front panel. The Off-Line command does not set Busy or Done.

SPACE FORWARD (command 3_g)

The controller advances the tape forward one or more records, but transfers no data. The number of records to be spaced over is determined by the contents of the C register. Spacing will continue until the C register overflows (increments to zero) or an End-of-File mark is encountered (an End-of-File mark is considered a record and increments the C register). The controller will go Busy for the duration of the operation and then go Done.

SPACE REVERSE (command 4₈)

The controller reverses the tape one or more records but does not transfer data. The number of records to be spaced over is determined by the contents of the C register. Spacing continues until either the C register overflows, the load point (BOT) marker is reached, or an end-of-file mark is encountered (the end-of-file mark will increment the C register). If the space reverse command is issued while the tape is at the End-of-Tape marker, the End-of-Tape status bit (S6) will not be set.

WRITE (command 5₈)

The controller places the addressed drive into the write mode and starts the tape in the forward direction. The controller writes the PE preamble and data on the tape. The memory location of the first data word written and the number of words to be written are determined by the contents of the B and C registers respectively. When the specified number of words have been transferred, the controller writes a postamble and erases a 0.6 inch gap (IRG) on the tape. The controller always writes an integral number of words from core with the shortest legitimate data record therefore consisting of two characters. The controller goes Busy for the duration of the transfer and goes Done when the transfer is complete. The PE identification burst will be automatically written if the tape is at the load point marker* when this command is executed.

- * Proper positioning of the identification burst relative to the load point marker requires that the tape be positioned at the load point by either a rewind command or a manual load operation.

WRITE EOF (command 6_g)

The controller starts the addressed drive, erases 3.5 inches of tape, writes an End-of-File mark and sets End-of-File status bit (S7). The PE identification burst will be written if the tape is at the load point marker* when this command is executed.

ERASE (command 7_g)

The controller erases 4 inches of tape on the addressed drive and then goes Done. The PE identification burst will be written if the tape is positioned at the load point marker* when this command is executed.

2.5 Nova Conventions

The 3180 controller responds to the following Nova instructions as outlined in the Nova Manual.

2.5.1 IORST Command

The IORST (I/O Reset) command resets the controller's A, B and C registers, all control logic and all status register bits not derived directly from the drive. Any operation in progress is terminated immediately, clearing both Busy and Done.

2.5.2 Interrupt Commands

The controller responds to INTA and MSKO commands. The mask bit is 10.

- * Proper positioning of the identification burst relative to the load point marker requires that the tape be positioned at the load point by either a rewind command or a manual load operation.

2.5.3 Flag Checking Commands

The controller responds to SKPBZ, SKPEN, SKPDZ and SKPDN commands addressed to device code 22₈ (MTA).

SECTION III - INSTALLATION

3.1 Scope

This section describes unpacking, inspection and installation procedures for the Model 3180 Phase Encoded Tape Drive Controller.

3.2 Unpacking and Inspection

Upon receipt of the controller from the carrier, inspect the two shipping cartons for external damage incurred during transit. Any indication of such damage must be noted by both the carrier and customer and should be reported to the insurance investigator immediately. Carefully unpack the shipping cartons and verify that the following items are included. The packaging material should be retained in case it should become necessary to reship the equipment at a later date.

Item 1: Tape controller logic card

Item 2: I/O Adapter Assembly and mounting hardware

Item 3: Two (2) controller-adapter interface cables

Item 4: Connector extractor tool (3M No. 3438)

Item 5: Documentation package including:

3180 Technical Manual

3180 Exerciser Manual and Tape

3180 Fault Locating Diagnostic Manual and Tape

3180 Magnetic Tape Drivers Manual and Tape

Complete set of logic schematics

Note: The contents of the documentation package varies with the recipient. Software items are normally supplied only initially with controllers shipped under OEM contracts.

Visually inspect each item for obvious physical damage. Verify that all items specified on both the purchase order and packing slip are included. If any items are missing or damaged, immediately contact the DECISION Field Service Representative or the factory.

3.3 Repacking For Shipment

If it should become necessary to return the equipment, contact your local DECISION Field Service Representative or the DECISION Field Service Department for shipping authorization. If possible, use the original packaging materials. If not available, the equipment should be packaged as follows:

1. Seal the logic card and adapter assembly in dust-proof, moisture-proof plastic bags.
2. To prevent damage in shipment, insulate the equipment with a type of cushioning packing material (e.g., convoluted foam or air-gap[®]).
3. Place the equipment in reinforced corrugated cartons and seal with strong packing tape.

3.4 Slide Mounted Rack Preparation

If the Nova computer is to be mounted in a standard RETMA rack on chassis slides, the right-side rack rail should be modified to prevent possible abrasion of the controller's input/output cables when the computer is slid in or out of the cabinet. Figure 3-1 illustrates the suggested sections to be removed for both the 5-1/4" and 10-1/2" Nova computer configurations. If the rack rails are removable, remove the right-side rail (as viewed from the front of the enclosure) and cut out the designated area. If the rails are an integral part of the enclosure, remove or adequately protect the equipment before cutting-out the

specified section. Deburr or file all rough edges. To permit adjustment of the slide rails from the front of the enclosure, enlarge the four holes (designated "A") and the corresponding holes on the left rack rail using a 7/32" drill bit.

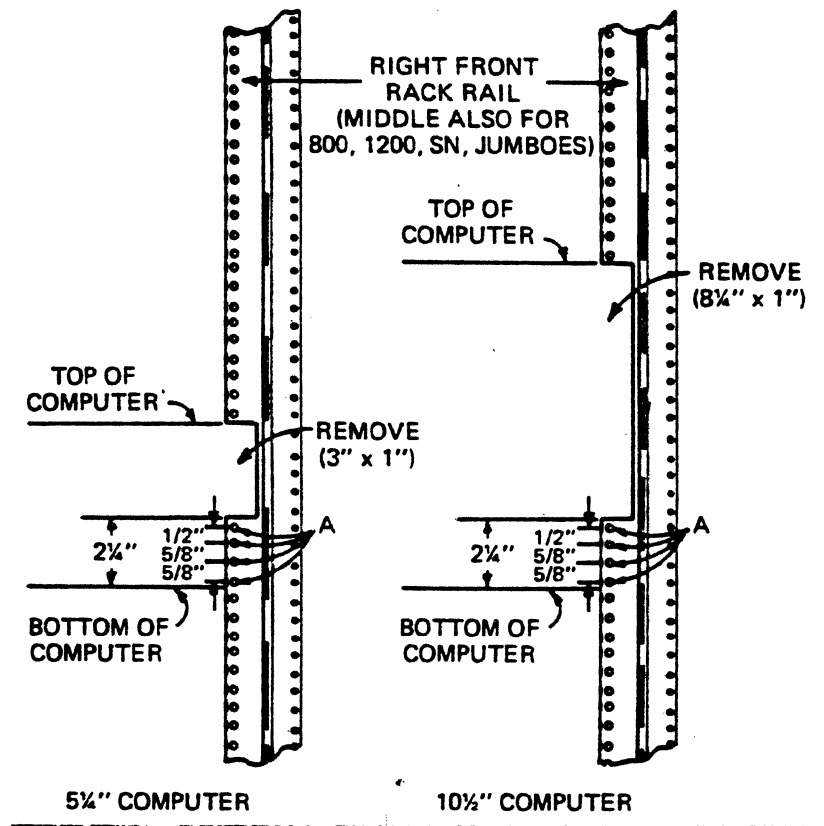


FIGURE 3-1

RACK RAIL MODIFICATION

3.5 Installation

Installation of the 3180 Controller involves installing the logic card into the CPU, installing the adapter assembly on/into the tape drive, interfacing the logic card to the adapter assembly and interfacing the adapter assembly to the tape drive. Before proceeding,

ensure that primary power is removed from both the CPU and tape drive. If the CPU has already been installed in the rack enclosure, slide the CPU out (if equipped with rack slides) or remove the CPU from the enclosure.

3.5.1 Logic Card

The logic card is designed to install directly into any Nova I/O subassembly slot. Unless the system employs another fast peripheral device such as a disk drive, A/D interface or high-speed communications interface, the 3180 logic card should occupy the highest priority I/O slot available (first position above the top memory board). Since the logic card is powered by the Nova's 5 volt supply, consideration should be made regarding the additional current requirement. Refer to Appendix B of "How to Use the Nova Computer" manual for power availability specifications for your specific Nova.

If, with the selection of the I/O slot, a vacant slot or slots exists between the top memory board and the logic card, the DCHP (Data Channel Priority) and INTP (INTerrupt Priority) signals must be physically jumpered on the Nova back plane to maintain priority interrupt continuity. The Nova back plane is accessible from the left side of the computer. Referring to the "Back Panel Connector Layout" illustration in Appendix A of the Nova manual, install one end of a wire-wrap jumper to the DCHP-OUT signal at pin 93 of the "A" connector (nearest the rear of the Nova) occupied by the device immediately below the logic card. Connect the remaining end to the DCHP-IN signal at pin 94 of the "A" connector occupied by the logic card, bridging the vacant slot or slots. Similarly, connect

the INTP-OUT signal (pin 95) from the lower device to the INTP-IN signal at pin 96 of the logic card's associated "A" connector.

This will complete the priority interrupt continuity to the logic card. If vacant slots exist between the logic card and the devices above the logic card, perform similar strapping of the DCHP and INTP signals to maintain interrupt priority.

If the logic card is to be installed in a Nova 800 Series or Supernova with the optional high-speed data channel, complete the wiring modifications outlined in Appendix A of the Nova manual to provide tape controller access to the high-speed channel.

The logic card should now be inserted, component side up, into the selected Nova I/O slot and locked in position with the release levers.

3.5.2 Adapter Assembly

The adapter assembly supplied is mounted either within or external to the tape drive depending on the drive manufacturer and model. Refer to the appropriate appendix at the conclusion of this manual for detailed mounting instructions for the specific drive.

3.5.3 Logic Card - Adapter Interface

After mounting the adapter assembly on the tape drive, the logic card-adapter interface cables should be installed. The logic card is fitted with two edge connectors, designated J1 and J2. Using one of the supplied interface cables (the cables are identical), connect one end of the cable to connector J2 on the logic card, arranging the cable to exit from the top of the connector as shown in Figure 3-2.

Mark the remaining end of this cable so it can be readily identified. Similarly, connect one end of the remaining cable to connector J1, again orienting the cable to exit from the top of the connector.

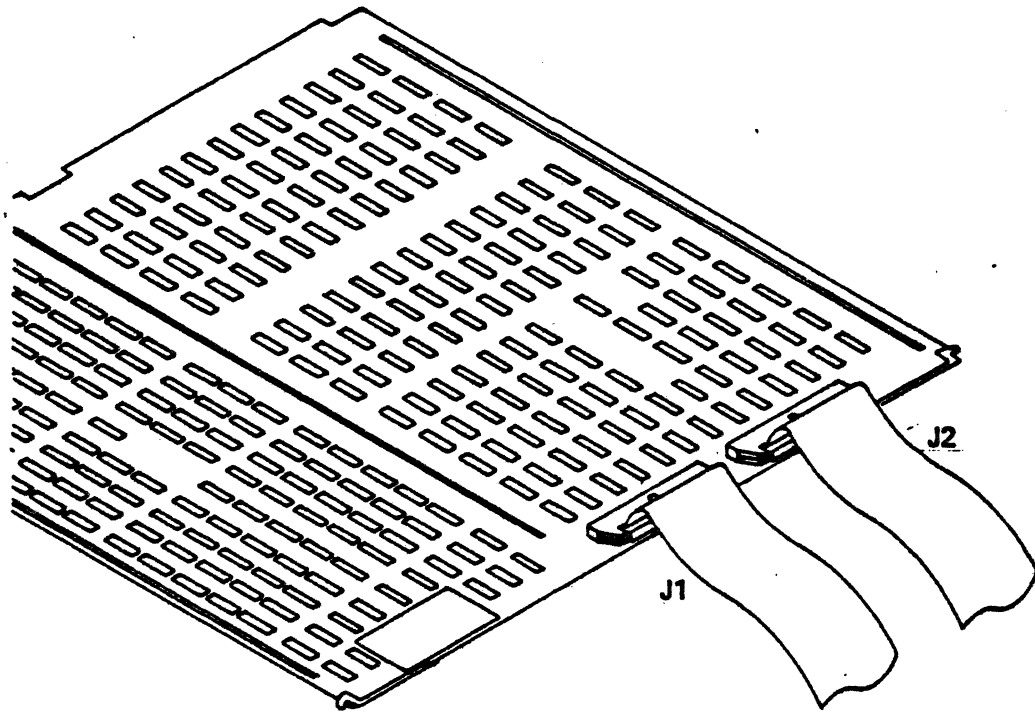


FIGURE 3-2
LOGIC CARD CONNECTORS

CAUTION

Never remove a cable from its connector by pulling on the cable directly. Use the supplied 3M Company "SCOTCHFLEX TOOL NO. 3438" or, if unavailable, alternately insert a small screwdriver into the slot on the top of the connector, twisting gently to separate.

After installing the cables, fold at 90° and route along the right side of the computer chassis to the rear of the computer as shown in Figure 3-3. Apply a small amount of adhesive to the inside of the fold to prevent the cables from protruding outwards and secure the cables to the chassis to ensure clearance between the computer and right-side of the enclosure. To secure the cables, use a strain relief (shown), strong tape, or Velcro®. It is important to secure the cables if the computer is mounted on rack slides.

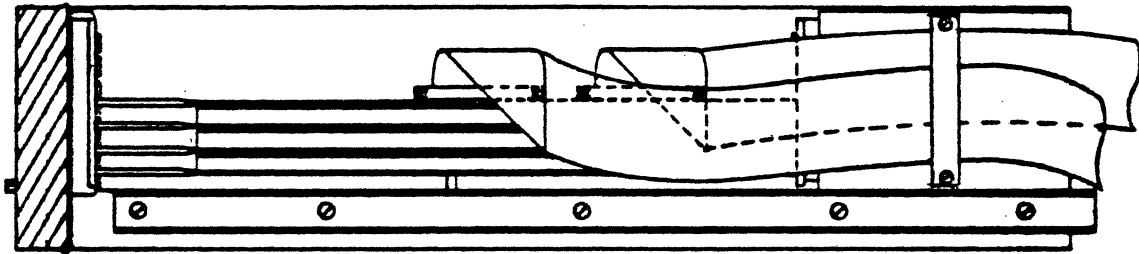


FIGURE 3-3

CABLE ROUTING

After securing the cables in place, the computer should be installed in the enclosure or slid into position, draping the cables down into the bottom of the enclosure.

Referring to Figure 3-4, connect the cable from connector J2 (previously marked) to connector I1 on the adapter assembly and connect the cable from connector J1 on the logic card to connector O1 on the adapter assembly.

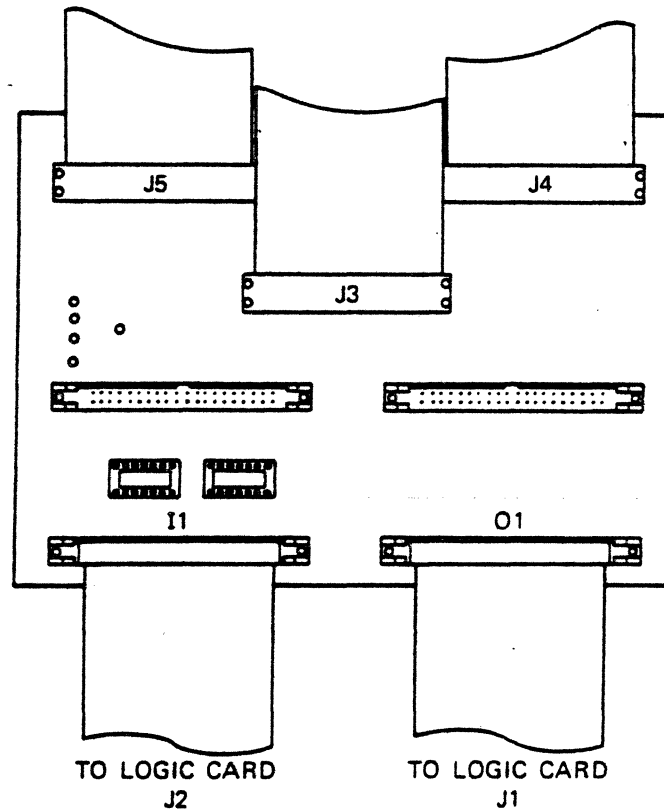


FIGURE 3-4

ADAPTER ASSEMBLY

3.5.4 Adapter-Drive Interface

The adapter assembly supplied incorporates three drive interface cables which are terminated with the proper mating connectors to interface directly with the type of drive specified. Refer to the appropriate appendix for detailed interface instructions for the type of drive used.

3.6 Multiple Drive Interface

Up to four tape drives can be interfaced to the Model 3180 Controller using a "daisy-chain" technique. The terminators in all but one drive must be removed. To connect multiple drives, interface the controller to the adapter assembly of the first drive as described in subsection 3.5.3. Connect one end of the daisy-chain cable to connector I2 on the first drive's adapter assembly. Connect the remaining end of this cable to connector I1 on the second drive's adapter assembly. Similarly, connect one end of another daisy chain cable to connector O2 on the first drive's adapter assembly and the remaining end to connector O1 on the second drive's adapter assembly. Continue this procedure for each drive in the system, providing terminators only in one drive.

After interfacing is complete, ensure that the drive select jumper on each adapter assembly is set to the correct drive number. Referring to the following illustration (Figure 3-5), the drive select cross-connect matrix is located at the center of the left-hand edge of the adapter card. Terminals 0, 1, 2, 3 correspond to the drive number. The drive is, in turn, selected by inserting a wire jumper between the desired unit number and terminal "S".

Note: Drive numbers may be assigned in random order. All drives within the same system must, however, be assigned a unique drive number.

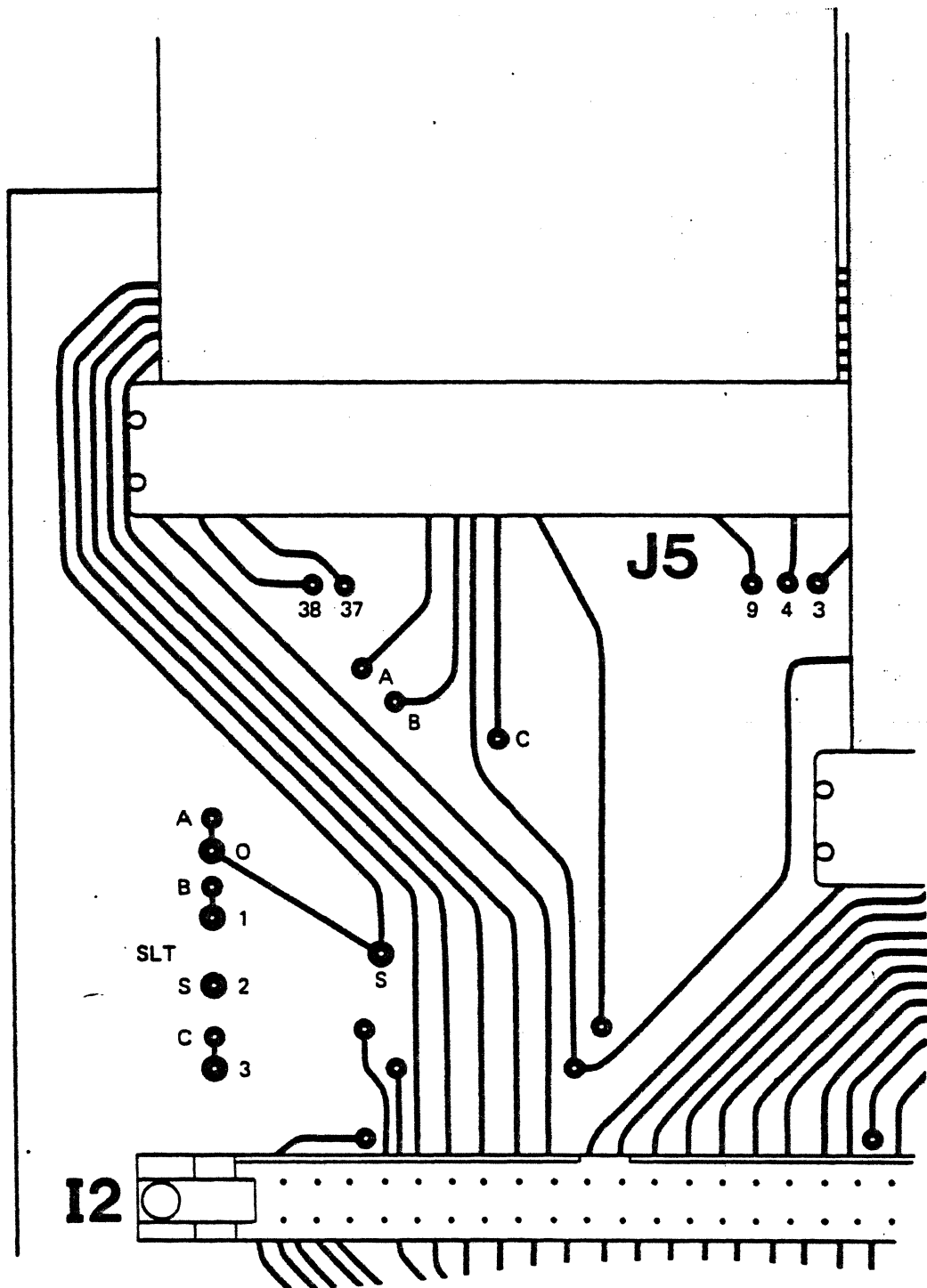


FIGURE 3-5

DRIVE SELECTION

APPENDICES

APPENDIX A

WANG MOD 10 AND MOD 11 INTERFACE

CABLE CONNECTION

Interface to the Wang Mod 10 or Mod 11 PE drives requires connecting the three cables from the adapter card to the corresponding connectors within the drive and installing the termination networks at the drive input cables. As shown in Figure A-1, the interface cables from the adapter card to the drive are labeled J3, J4, and J5. The remaining ends of these cables are fitted with the appropriate mating connectors for the Wang drives.

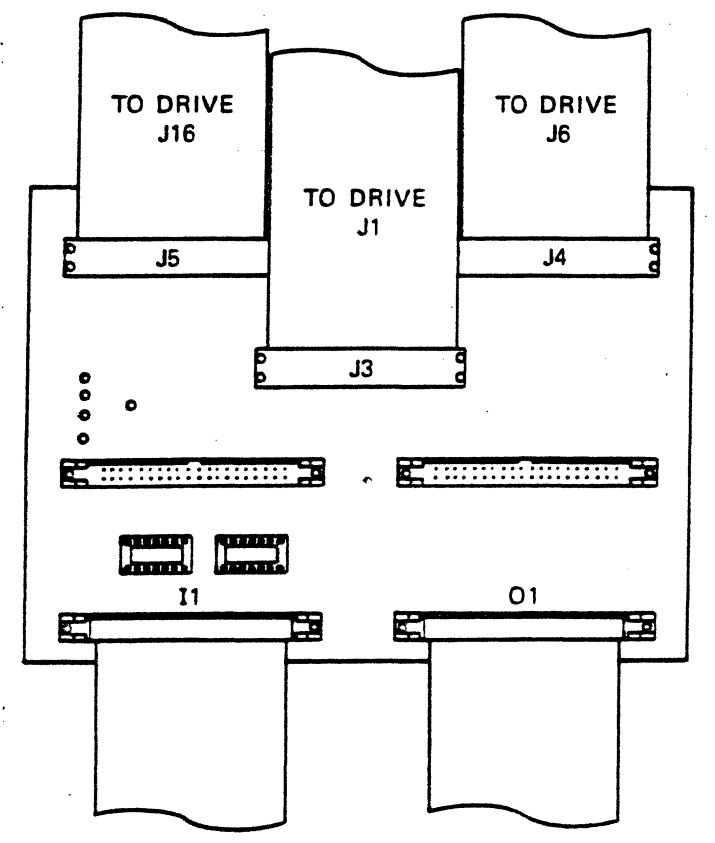


FIGURE A-1
ADAPTER CARD

Referring to Figure A-2 (Mod 10) or Figure A-3 (Mod 11), there are three sets of drive interface connectors labeled P1 (A and B), P6 (A and B) and P16 (A and B). Each set is identical, pin-for-pin, permitting the corresponding cable from the adapter card to be installed on either the "A" or "B" connector. Referring to the following table, connect the cables from the adapter card to the tape drive as noted, referencing pin A on the drive connector with pin A of the cable connector.

ADAPTER CARD CABLE	DRIVE CONNECTOR	FUNCTION
J3	P1 (A or B)	Write Data
J4	P6 (A or B)	Read Data
J5	P16 (A or B)	Drive Control and Status

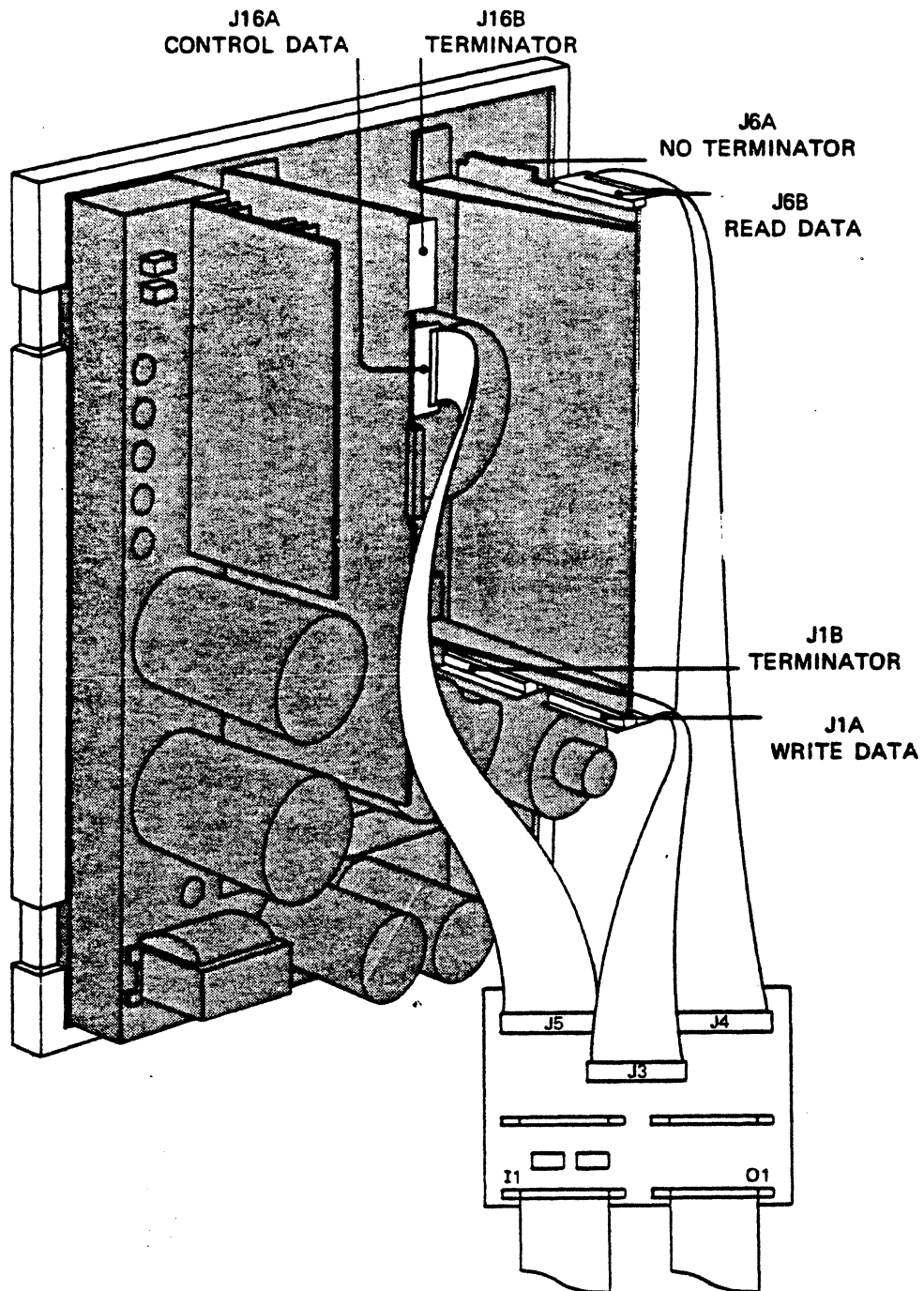


FIGURE A-2
MOD 10 DRIVE CABLE INTERFACE

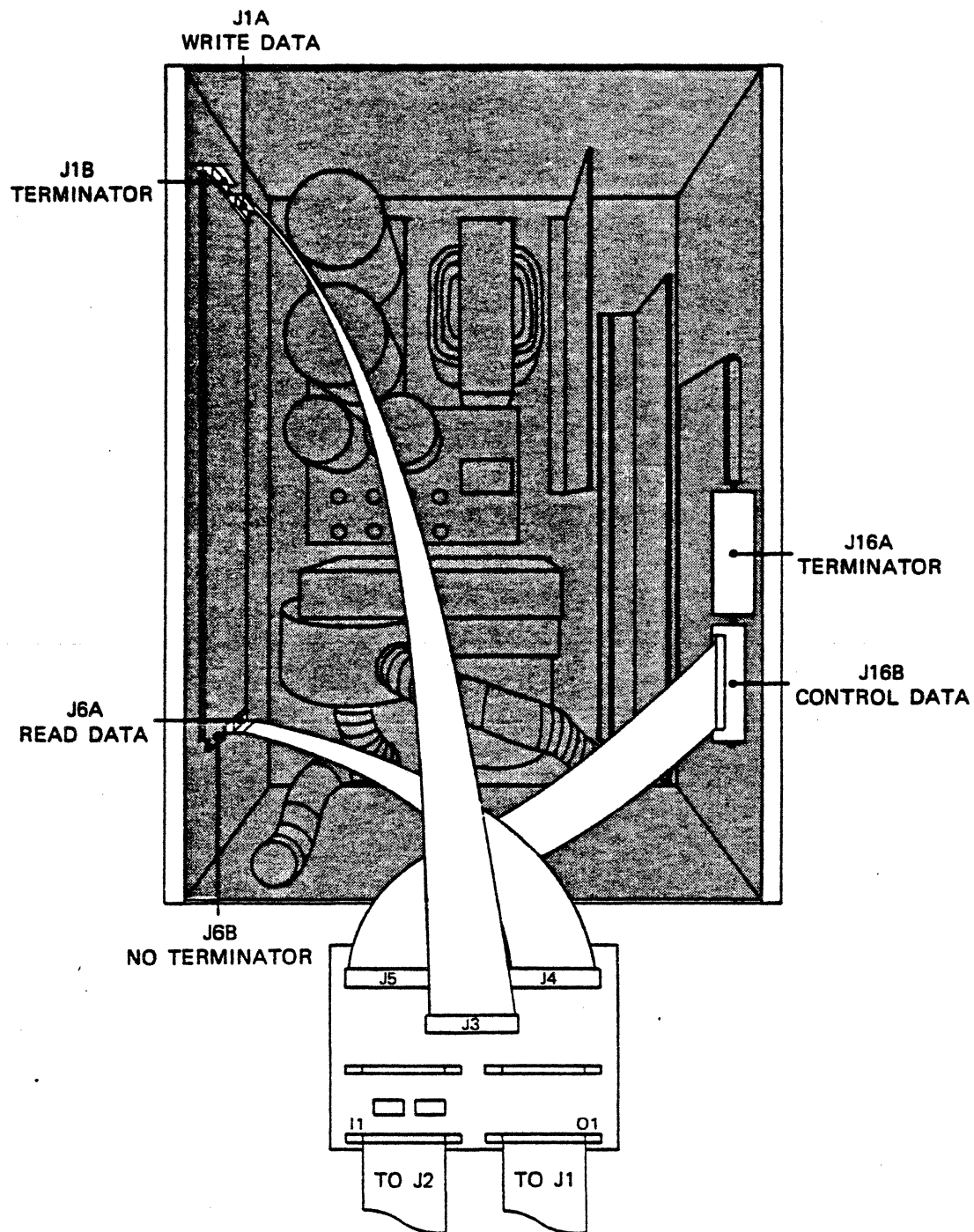


FIGURE A-3
MOD 11 DRIVE CABLE INTERFACE

TERMINATORS

If only one drive is to be interfaced to the controller, install the Wang terminator boards (supplied with the drive) on the vacant connector locations at P1 and P16 ONLY.

NOTE

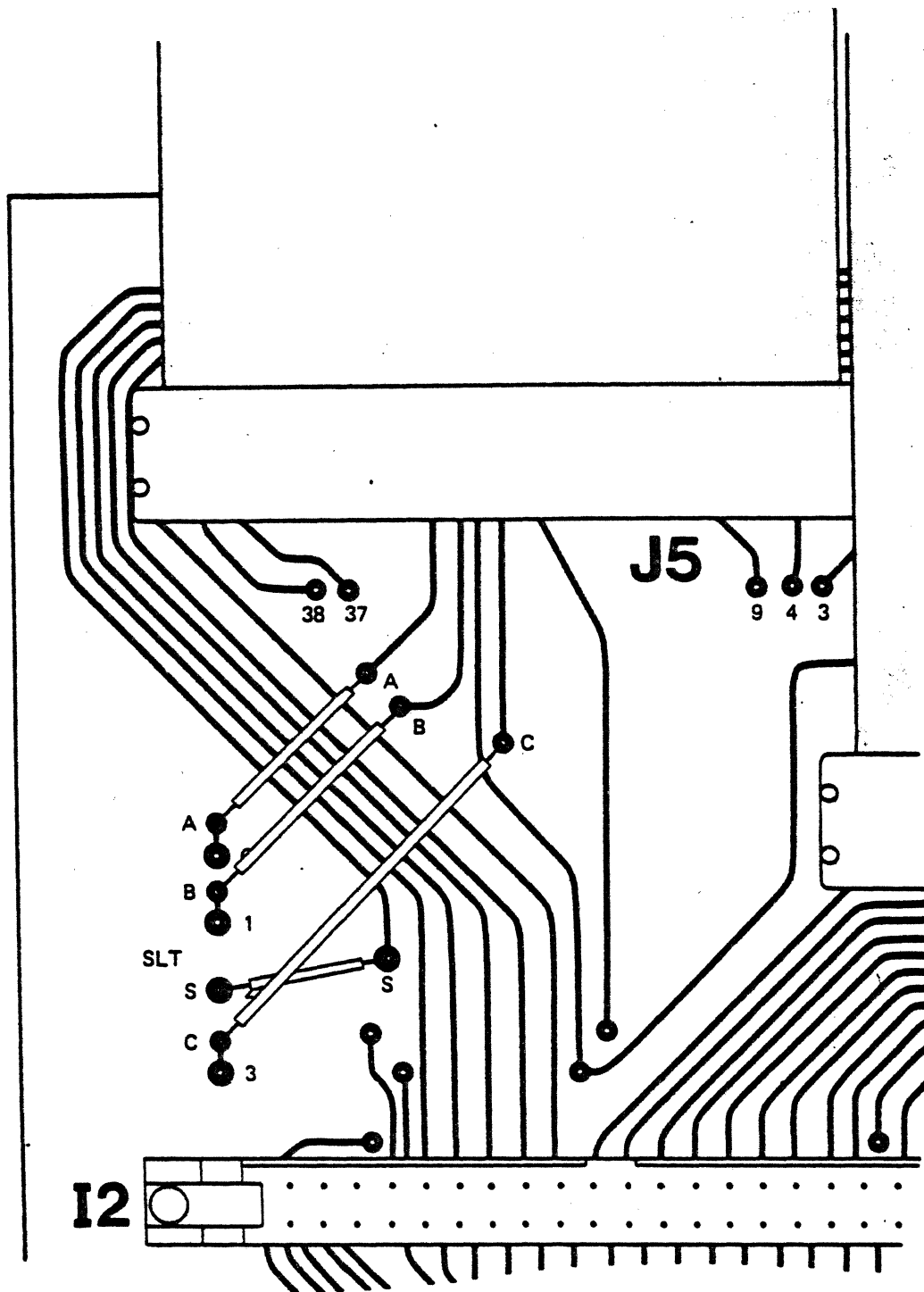
Do not install a terminator at connector location P6. These lines (read data) are terminated on the controller logic card.

If more than one drive is to be interfaced (daisy chained) to the controller, terminators are installed (at P1 and P16) only on one drive.

When the adapter card termination networks are to be used in place of the drive terminators, install a resistor package (Beckman 899-5-220/330 or equivalent) at locations IC1 and IC2 on the board. Vcc to the resistor packages is supplied from the drive.

DRIVE OPTIONS

If the Wang drive incorporates the optional remote unit select switch, the adapter card drive select cross connect must be modified. Referring to Figure A-4, install jumpers between pads A and A, B and B, C and C, and S and S as shown to enable drive selection by the remote switch.



A-4

UNIT SELECT SWITCH MODIFICATION

A-6

SCHEMATICS AND RELATED DRAWINGS

**3180 STATE/MODE
DEFINITION TABLE**

STATE	FUNCTION	EXIT CONDITION
①	INITIAL BRANCH STATE	OVF
①	READ START DELAY	OVF
②	ERASE 4 INCH GAP	OVF
③	WRITE PE ID BURST	OVF
④	WRITE TAPE MARK	OVF
⑤	WRITE PREAMBLE	OVF
⑥	WRITE DATA BLOCK	Both Buffers Empty
⑦	WRITE POSTAMBLE	OVF
⑧	ERASE 2 INCH GAP	OVF
⑨	ENABLE READ CIRCUITS	OVF
⑩	WRITE START DELAY	OVF
⑪	RAMP DOWN TIME DELAY	OVF
⑫	POST RECORD DELAY	OVF
⑬	AWAIT EOR (End Of Record)	EOR or BOT Detected

OVF = State Duration Counter Overflow

The State/Mode table (above) and the individual operation step/flow diagrams on the succeeding pages, define the individual functions associated with the selected operation and the condition causing the controller to advance to the next logical step.

**WRITE OPERATION
(Not at BOT)**



**WRITE OPERATION
(At BOT)**



READ OPERATION



NOTE: Duration of state 1 in read mode is determined by position of tape relative to BOT.

**ERASE
(Not at BOT)**



**ERASE
(At BOT)**



SPACE FORWARD



NOTE: Duration of state 1 in space forward mode is determined by the position of the tape relative to the BOT.

SPACE REVERSE
(Not at BOT)



WRITE EOF
(Not at BOT)



WRITE EOF
(At BOT)



ACRONYM	NAME	ORIGIN	DESTINATION
B1 CLOCK	Buffer 1 Clock	7	14
B3DAT0-B3DAT15	Buffer 3 Data 0-15	14	6,30
BRANCH	Branch	4	3
BUFF CLOCK	Buffer Clock	7	11,12,14,24
BUFFO P	Buffer Overflow Channel P	15	10
BUFFO 0	Buffer Overflow Channel 0	16	10
BUFFO 1	Buffer Overflow Channel 1	17	10
BUFFO 2	Buffer Overflow Channel 2	18	10
BUFFO 3	Buffer Overflow Channel 3	19	10
BUFFO 4	Buffer Overflow Channel 4	20	10
BUFFO 5	Buffer Overflow Channel 5	21	10
BUFFO 6	Buffer Overflow Channel 6	22	10
BUFFO 7	Buffer Overflow Channel 7	23	10
BXBUSY	Buffer X Busy	11	3,12,24
BXBUSY	Buffer X Busy	11	12
BYBUSY	Buffer Y Busy	11	12
BYBUSY	Buffer Y Busy	11	12,24
CBRP	Character Buffer Register Bit P	13	10
CBR0-CBR7	Character Buffer Register 0-7	13	10,14
CFREQ	Character Frequency	7	31
CH1 TRANS	Channel 1 Transition	17	31
CH2 BIT	Channel 2 Bit	18	8
CH2 TRANS	Channel 2 Transition	18	31
CH3 TRANS	Channel 3 Transition	19	31
CH4 TRANS	Channel 4 Transition	20	31
CH6 TRANS	Channel 6 Transition	22	31
CLR	Clear	CPU	28
CLRFLAG	Clear Flag	28	9,10,12,26,31
COMMAND 0	Command Bit 0	26	3
COMMAND 1	Command Bit 1	26	3
COMMAND 2	Command Bit 2	26	3
CORINIT	Clear Or Initialize	28	25,26

ACRONYM	NAME	ORIGIN	DESTINATION
<u>DATA0-15</u>	Data 0-15	32	CPU
<u>DATIA</u>	Data In A	CPU	30
<u>DATIB</u>	Data In B	CPU	30
<u>DATIC</u>	Data In C	CPU	30
<u>DATOA</u>	Data Out A	CPU	26
<u>DATOB</u>	Data Out B	CPU	29
<u>DATOC</u>	Data Out C	CPU	29
<u>DCHA</u>	Data Channel Acknowledge	CPU	24
<u>DCHAD0-14</u>	Data Channel Address 0-14	29	30
<u>DCHI</u>	Data Channel In	CPU	24
<u>DCHIN</u>	Data Channel In	24	11,30
<u>DCHM0</u>	Data Channel Mode 0	24	CPU
<u>DCHO</u>	Data Channel Out	CPU	24
<u>DCHOUT</u>	Data Channel Out	24	7,11
<u>DCHP IN</u>	Data Channel Priority In	CPU	24
<u>DCHP OUT</u>	Data Channel Priority Out	24	CPU
<u>DCHR</u>	Data Channel Request	24	CPU
<u>DLATES</u>	Data Late Status	12	30
<u>DLATES</u>	Data Late Status	12	25
<u>DPETBUSY</u>	Delayed PE Tape Busy	28	24
<u>DPETBUSY</u>	Delayed PE Tape Busy	28	26
<u>DROP P</u>	Dropped Bit Channel P	15	10
<u>DROP 0</u>	Dropped Bit Channel 0	16	10
<u>DROP 1</u>	Dropped Bit Channel 1	17	10
<u>DROP 2</u>	Dropped Bit Channel 2	18	10
<u>DROP 3</u>	Dropped Bit Channel 3	19	10
<u>DROP 4</u>	Dropped Bit Channel 4	20	10
<u>DROP 5</u>	Dropped Bit Channel 5	21	10
<u>DROP 6</u>	Dropped Bit Channel 6	22	10
<u>DROP 7</u>	Dropped Bit Channel 7	23	10
<u>DS0-5</u>	Device Select 0-5	CPU	28
<u>ENAREAD</u>	Enable Read	3	4
<u>ENA 134</u>	Enable Channels 1,3 and 4	3	6
<u>ENA 02567</u>	Enable Channels 0,2,5,6 and 7	3	6

ACRONYM	NAME	ORIGIN	DESTINATION
EORDET	End Of Record Detected	31	4,29
<u>EORDET</u>	End Of Record Detected	31	4
<u>EOT</u>	End Of Tape	Drive	26
EOTS	End Of Tape Status	26	30
<u>EOTS</u>	End Of Tape Status	26	25
<u>ERASEC</u>	Erase Command	26	4
<u>ERA4GAP</u>	Erase 4 Inch Gap	3	4,31
ERRORS	Error Status	25	30
EWCOO	Error Word Count OO	29	30
EWCO-2	Error Word Count O-2	29	30
EWST	Enable Write Strobe	3	6
<u>FINISHED</u>	Finished	4	28
FIX CLOCK	Fixed Frequency Clock	7	3,4,5,6,25,28,31
FM TEST	File Mark Test	8	31
<u>FPT</u>	File Protect	Drive	26
FSTATE O	Function State O	3	5
FSTATE 1	Function State 1	3	5
FSTATE 2	Function State 2	3	5
FSTATE 3	Function State 3	3	5
<u>FSTSTA</u>	First State	8	31
FULL	Word Count Full	29	4,12
<u>FULL</u>	Word Count Full	29	24
IDATAO	In Data O	32	14
IDATA1-4	In Data 1-4	32	14,29
IDATA5	In Data 5	32	14,26,29
IDATA6-8	In Data 6-8	32	14,29
IDATA9	In Data 9	32	14,26,29
IDATA10	In Data 10	32	14,26,28,29
IDATA11,12	In Data 11,12	32	14,26,29
IDATA13	In Data 13	32	14,29
IDATA14,15	In Data 14,15	32	14,26,29
ILLEGALS	Illegal Status	26	30
<u>ILLEGALS</u>	Illegal Status	26	25

ACRONYM	NAME	ORIGIN	DESTINATION
<u>ILL STAR</u>	Illegal Start	26	28
<u>INIT</u>	Initialize	32	24,26,28,29
<u>INTA</u>	Interrupt Acknowledge	CPU	28
<u>INTP IN</u>	Interrupt Priority In	CPU	28
<u>INTP OUT</u>	Interrupt Priority Out	27	CPU
<u>INTR</u>	Interrupt Request	28	CPU
<u>IORST</u>	I/O Reset	CPU	32
<u>IRQENB</u>	Interrupt Request Enable	28	24
<u>LADDR</u>	Load Address	24	29,30
<u>LAR</u>	Load Address Register	9	10
<u>LCCRY</u>	Last Count Carry	8	31
<u>LDP</u>	Load Point	Drive	26
<u>LOADB1L</u>	Load Buffer 1 LSB	9	14
<u>LOADB1M</u>	Load Buffer 1 MSB	9	14
<u>LOADB2</u>	Load Buffer 2	11	14
<u>LOADB3</u>	Load Buffer 3	11	14
<u>LOADFORM</u>	Load Format	3	5
<u>LOADPOINTS</u>	Load Point Status	26	3,30
<u>LOADPOINTS</u>	Load Point Status	26	4,25
<u>LOCKREF</u>	Lock Reference	8	7
<u>LOW THRESHOLD</u>	Low Threshold	26	Drive
<u>MDENS</u>	Multiple Density	CPU	27
<u>MIDPOST</u>	Middle Of Postamble	8	12
<u>MSKO</u>	Mask Out	CPU	28
<u>NORMSTAR</u>	Normal Start	26	25,28
<u>ODATA0-9</u>	Out Data 0-9	30	32
<u>ODATA10,11</u>	Out Data 10,11	28,30	32
<u>ODATA12,13</u>	Out Data 12,13	30	32
<u>ODATA14</u>	Out Data 14	28,30	32
<u>ODATA15</u>	Out Data 15	30	32
<u>ODDCHARS</u>	Odd Character Status	9	30
<u>ODDCHARS</u>	Odd Character Status	9	25

ACRONYM	NAME	ORIGIN	DESTINATION
<u>ODDPAR</u>	Odd Parity	26	6,10
<u>ODDPAR</u>	Odd Parity	26	6,10
<u>ODDZERO</u>	Odd Zero	9	14
<u>OFFCD</u>	Off-Line Command Drive	25	Drive
<u>OFFLINEC</u>	Off-Line Command	26	25,28
<u>OVFLOW</u>	Overflow	5	3,4
<u>P ERRORS</u>	Parity Error Status	10	30
<u>P ERRORS</u>	Parity Error Status	10	25
<u>PETBUSY</u>	PE Tape Busy	28	3,4,5,6,11,12,26,29,31
<u>PETSEL</u>	PE Tape Select	27	26,28,30
<u>PETSELX</u>	PE Tape Selected	28	26,27,29
<u>PETSTAR</u>	PE Tape Start	26	3,28
<u>PHASE</u>	Phase	5	6
<u>PLLCLOCK 1</u>	Phase Lock Loop Clock 1	7	15
<u>PLLCLOCK 2</u>	Phase Lock Loop Clock 2	7	16,21,22,23
<u>PLLCLOCK 3</u>	Phase Lock Loop Clock 3	7	13,21,23
<u>PLLCLOCK 4</u>	Phase Lock Loop Clock 4	7	17,18
<u>PLLCLOCK 5</u>	Phase Lock Loop Clock 5	7	9,19,20
<u>PLLCLOCK 6</u>	Phase Lock Loop Clock 6	7	21,22,23
<u>PLLCLOCK 7</u>	Phase Lock Loop Clock 7	7	16,22
<u>PLLCLOCK 8</u>	Phase Lock Loop Clock 8	7	18,19,20
<u>PLLCLOCK 9</u>	Phase Lock Loop Clock 9	7	17
<u>PLLCLOCK 10</u>	Phase Lock Loop Clock 10	7	8,9
<u>PLLCLOCK 11</u>	Phase Lock Loop Clock 11	7	8,10,31
<u>PLLLOCKED 1</u>	Phase Lock Loop Locked 1	8	9,10,17,18,19,20
<u>PLLLOCKED 2</u>	Phase Lock Loop Locked 2	8	15,16,21,22,23
<u>POSTAMBLEP</u>	Postamble Pulse	13	9,10
<u>POST D</u>	Postamble Detected	9	8
<u>POST D</u>	Postamble Detected	9	8
<u>POSTRECDEL</u>	Post Record Delay	3	4,31
<u>PPFW1</u>	{ Preamble Postamble Filemark Write 1	3	6
<u>PPFW1</u>		3	6

ACRONYM	NAME	ORIGIN	DESTINATION
QB	Phase B	5	6
QC	Phase C	5	6
<u>RAMPOVER</u>	Ramp Over	3	4
<u>RDY</u>	Ready	Drive	26
READC	Read Command	26	8,9,11,24
<u>READC</u>	Read Command	26	3,9,14
READYS	Ready Status	26	30
<u>REWINDC</u>	Rewind Command	26	25,28
REWINDS	Rewind Status	26	30
<u>RDP</u>	Read Data Parity	Drive	15
<u>RD 0</u>	Read Data 0	Drive	16
<u>RD 1</u>	Read Data 1	Drive	17
<u>RD 2</u>	Read Data 2	Drive	18
<u>RD 3</u>	Read Data 3	Drive	19
<u>RD 4</u>	Read Data 4	Drive	20
<u>RD 5</u>	Read Data 5	Drive	21
<u>RD 6</u>	Read Data 6	Drive	22
<u>RD 7</u>	Read Data 7	Drive	23
RLOABR	Reload Buffer Register	9	11,12
RLOADB	Reload Character Buffer	9	13,15,16,17,18,19, 20,21,22,23
<u>RWD</u>	Rewind	Drive	26
<u>RLOADB</u>	Reload Buffer	9	13
<u>RQENB</u>	Request Enable	CPU	28
<u>RRES 1</u>	Read Reset 1	4	8
<u>RRES 2</u>	Read Reset 2	4	8
<u>RSD</u>	Read Strobe Delay	3	31
<u>RWCD</u>	Rewind Command Drive	25	Drive
SBOT	Beginning Of Tape Status	3	5
SCLOCK	Send Clock	31	30
SECSTA	Second State	8	31
<u>SELB</u>	Select Busy	28	CPU
<u>SELD</u>	Select Done	28	CPU

ACRONYM	NAME	ORIGIN	DESTINATION
<u>SELFIX</u>	Select Fixed Clock	8	7
<u>SELFIX</u>	Select Fixed Clock	8	7,30
<u>SELMSB</u>	Select Most Significant Bit	5	6
<u>SET TAPE ERRORS</u>	Set Tape Error Status	3	10
<u>SFCD</u>	Stop/Forward Command Drive	25	Drive
<u>SHUT OFF</u>	Shut Off	4	25
<u>SKBB P</u>	Skew Buffer Busy P	15	9
<u>SKBB Ø</u>	Skew Buffer Busy Ø	16	9
<u>SKBB 1</u>	Skew Buffer Busy 1	17	9
<u>SKBB 2</u>	Skew Buffer Busy 2	18	9
<u>SKBB 3</u>	Skew Buffer Busy 3	19	9
<u>SKBB 4</u>	Skew Buffer Busy 4	20	9
<u>SKBB 5</u>	Skew Buffer Busy 5	21	9
<u>SKBB 6</u>	Skew Buffer Busy 6	22	9
<u>SKBB 7</u>	Skew Buffer Busy 7	23	9
<u>SKDATA P</u>	Skew Data P	15	13
<u>SKDATA Ø</u>	Skew Data Ø	16	13
<u>SKDATA 1</u>	Skew Data 1	17	13
<u>SKDATA 2</u>	Skew Data 2	18	13
<u>SKDATA 3</u>	Skew Data 3	19	13
<u>SKDATA 4</u>	Skew Data 4	20	13
<u>SKDATA 5</u>	Skew Data 5	21	13
<u>SKDATA 6</u>	Skew Data 6	22	13
<u>SKDATA 7</u>	Skew Data 7	23	13
<u>SLCT Ø</u>	Select Bit Ø	26	27
<u>SLCT 1</u>	Select Bit 1	26	27
<u>SLTDØ-3</u>	Select Drive Bits Ø-3	27	Drive
<u>SMOTION</u>	Start Motion	28	25
<u>SPACE</u>	Space	29	4
<u>SPFC</u>	Space Forward Command	26	29
<u>SPRC</u>	Space Reverse Command	26	25
<u>SPRC</u>	Space Reverse Command	26	25,29
<u>SRCD</u>	Stop/Reverse Command Drive	25	Drive
<u>STER</u>	Set Tape Error	10	8

ACRONYM	NAME	ORIGIN	DESTINATION
STRT	Start	CPU	26
<u>SWSD</u>	Write Enable Drive	26	Drive
<u>SYNCDP</u>	Synchronized Data Channel	11	12,24
TCX	Terminal Count	5	3
T ERRORS	Tape Error Status	10	30
<u>T ERRORS</u>	Tape Error Status	10	25
TMARKS	Tape Mark Status	31	4,8,30
<u>TMARKS</u>	Tape Mark Status	31	25
<u>WBLOCK</u>	Write Block	3	5
WC0-11	Word Count 0-11	29	30
<u>WDP</u>	Write Data Parity Bit	6	Drive
<u>WD0-7</u>	Write Data Bits 0-7	6	Drive
WID	Write ID Burst	3	6
<u>WID</u>	Write ID Burst	3	6
WLOCKS	Write Lock Status	26	30
WRITE 1	Write 1	3	6
WRITEC	Write Command	26	7,9,11,24
<u>WRITEC</u>	Write Command	26	4,5,7
WRITE COM	Write Common	26	3,6
<u>WSTARDLY</u>	Write Start Delay	3	31
<u>WUNLOADBR</u>	Write Unload Buffer Register	5	3,11,12

CONFIDENTIAL INFORMATION

The design, information, and data contained herein is proprietary and is submitted in confidence, and shall not be disclosed, used, or duplicated, in whole or in part, for any purpose whatsoever without prior written permission of Ball Computer Products, Inc. 3401 College Avenue, Oakland, California 94612. This legend shall be marked on any reproduction hereof in whole or in part. Receipt of this document shall be deemed to be an acceptance of the conditions specified herein.

LTR	DESCRIPTION	DATE	APP
A	DOC. RELEASE EO. 1124	3-24-74	K.P.
B	REF EO. 1161	11-11-74	—
C	REF EO. 1176	11-10-74	—
D	REF EO. 1352	4-22-75	D.R.
E	REF EO. 1481	9-18-75	—
F	REF E.O. 14176	10-21-76	—

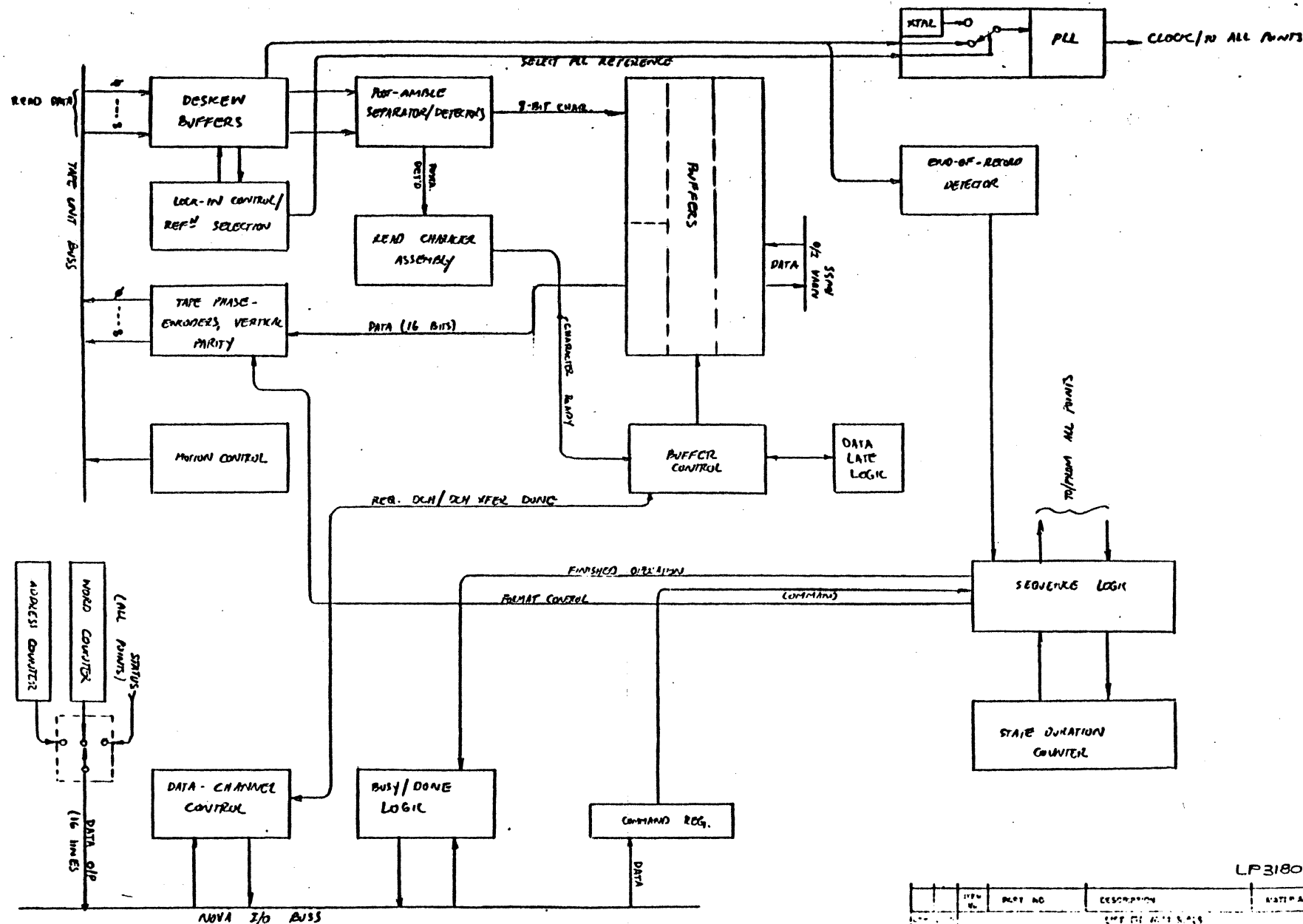
SHEET

TITLE

- 2 ELEMENTARY DIAGRAM
- 3 FORMAT CONTROL LOGIC (SECTION I)
- 4 FORMAT CONTROL LOGIC (SECTION II)
- 5 STATE DURATION COUNTER
- 6 TAPE PHASE ENCODERS, WRITE VERTICAL PARITY
- 7 CLOCK SWITCHING MASTER OSCILLATOR TRACKING OSCILLATOR
- 8 LOCK-IN CONTROL REFERENCE SELECTION
- 9 READ CHARACTER ASSEMBLY
- 10 TAPE ERROR SENSING VERTICAL PARITY CHECK
- 11 BUFFER CONTROL
- 12 "DATA-LATE" LOGIC
- 13 POST-AMBLE SEPERATOR POST-AMBLE DETECTORS
- 14 CHANNEL BUFFERS
- 15 CHANNEL P DESKEWING BUFFER
- 16 CHANNEL 0 DESKEWING BUFFER
- 17 CHANNEL 1 DESKEWING BUFFER
- 18 CHANNEL 2 DESKEWING BUFFER
- 19 CHANNEL 3 DESKEWING BUFFER
- 20 CHANNEL 4 DESKEWING BUFFER
- 21 CHANNEL 5 DESKEWING BUFFER
- 22 CHANNEL 6 DESKEWING BUFFER
- 23 CHANNEL 7 DESKEWING BUFFER
- 24 DATA-CHANNEL CONTROL
- 25 TRANSPORT MOTION CONTROL STATUS LOGIC
- 26 TAPE TRANSPORT STATUS COMMAND DECODER
- 27 UNIT SELECT LOGIC
- 28 "NOVA" COMPUTER INTERFACE
- 29 WORD COUNTERS ADDRESS COUNTERS
- 30 DATA OUTPUT SWITCH STATUS OUTPUT
- 31 TAPE-MARK DETECTOR BLOCK-GAP DETECTORS
- 32 "NOVA" COMPUTER DATA LINES I/O

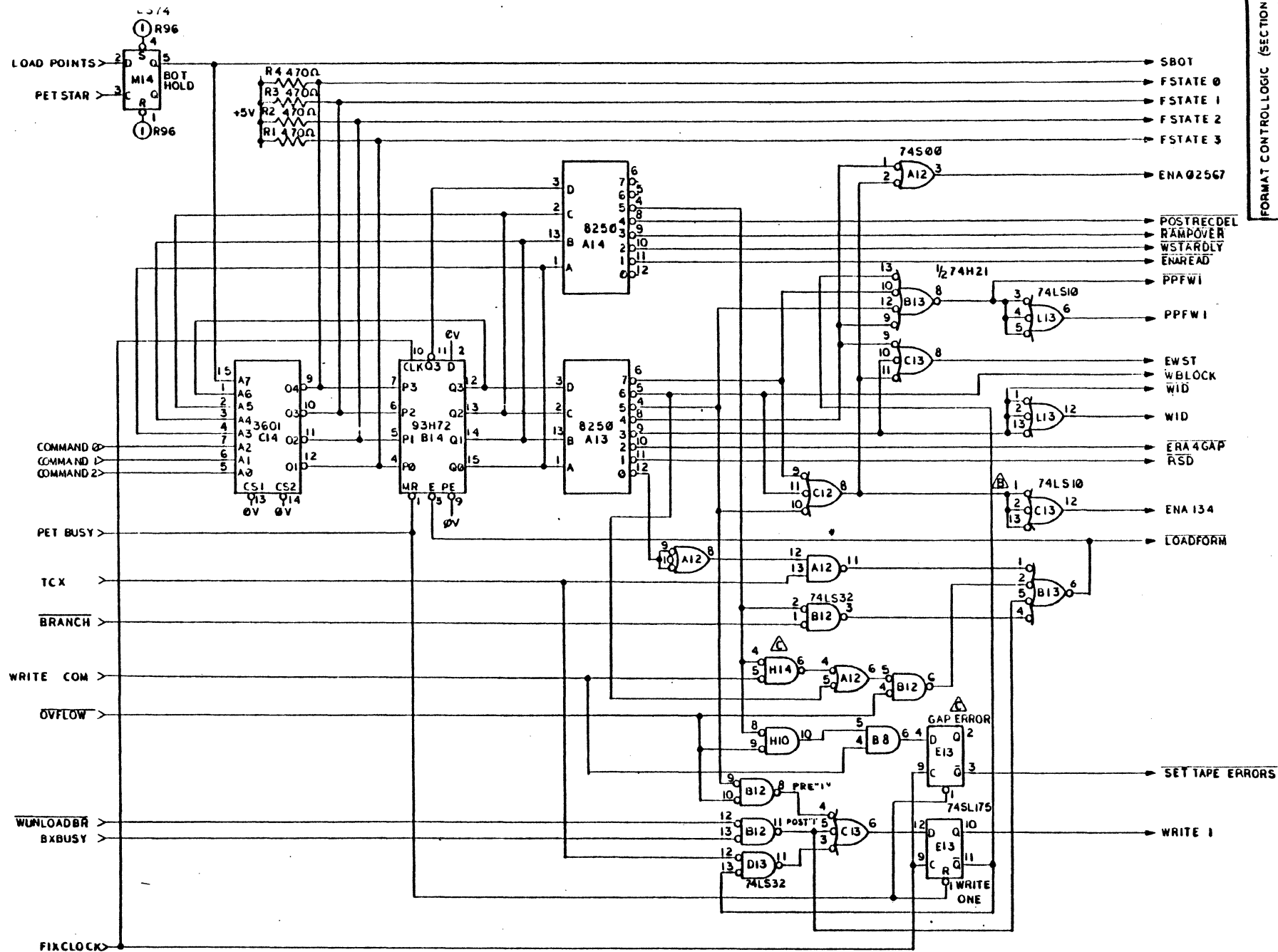
UNIT PHASE ENCODED TAPE		 Ball Computer Products, Inc. OAKLAND, CA 94612
92-0003124-0	DATE	
96-0903161-2	DRAWN R. WILSON	
96-0903160-0	CHECK	
96-0903157-1	DESIGN	
91-0203445-2	R. WILSON	SCHEMATIC, 3180 TAPE CONTROLLER
91-0203125-5	APR BY R.D.	
SIZE DWE. NO.		96-0203474-7 F

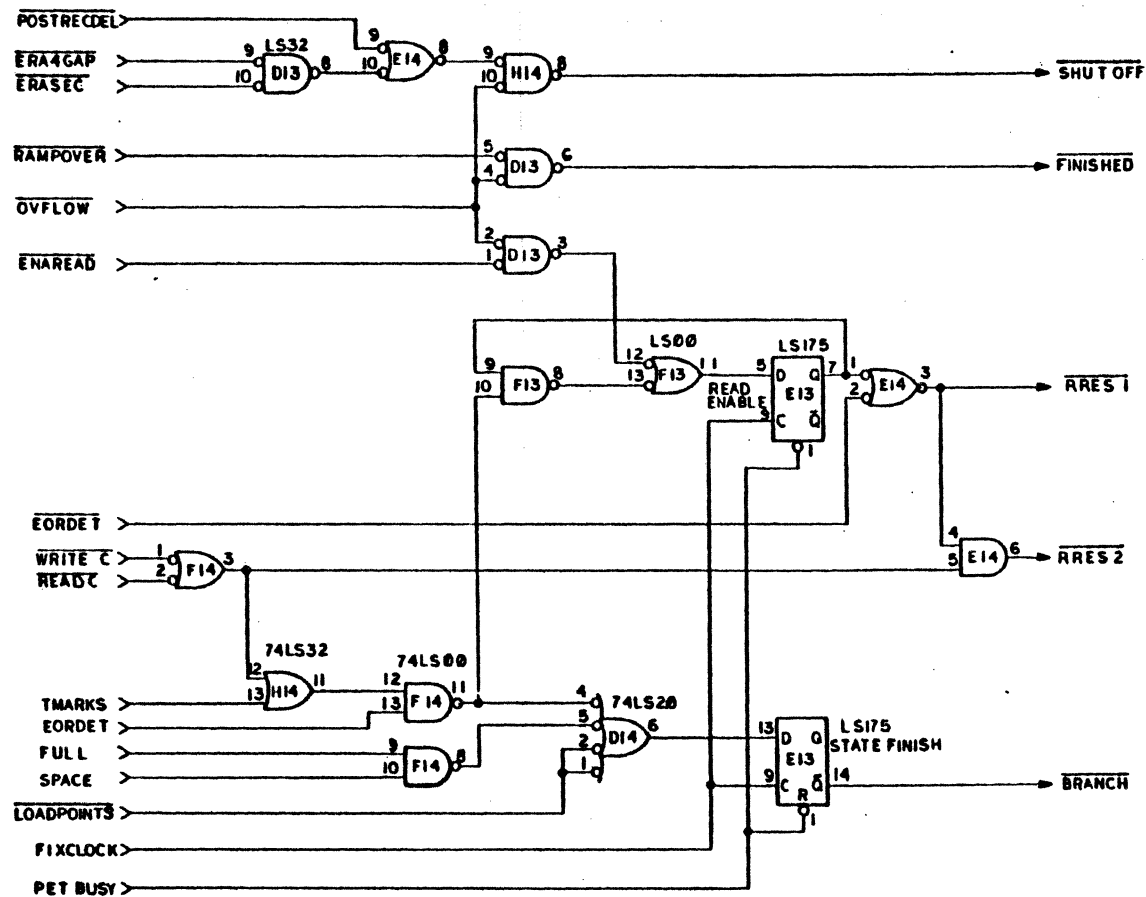
DATE REC 96-0203474-7 E

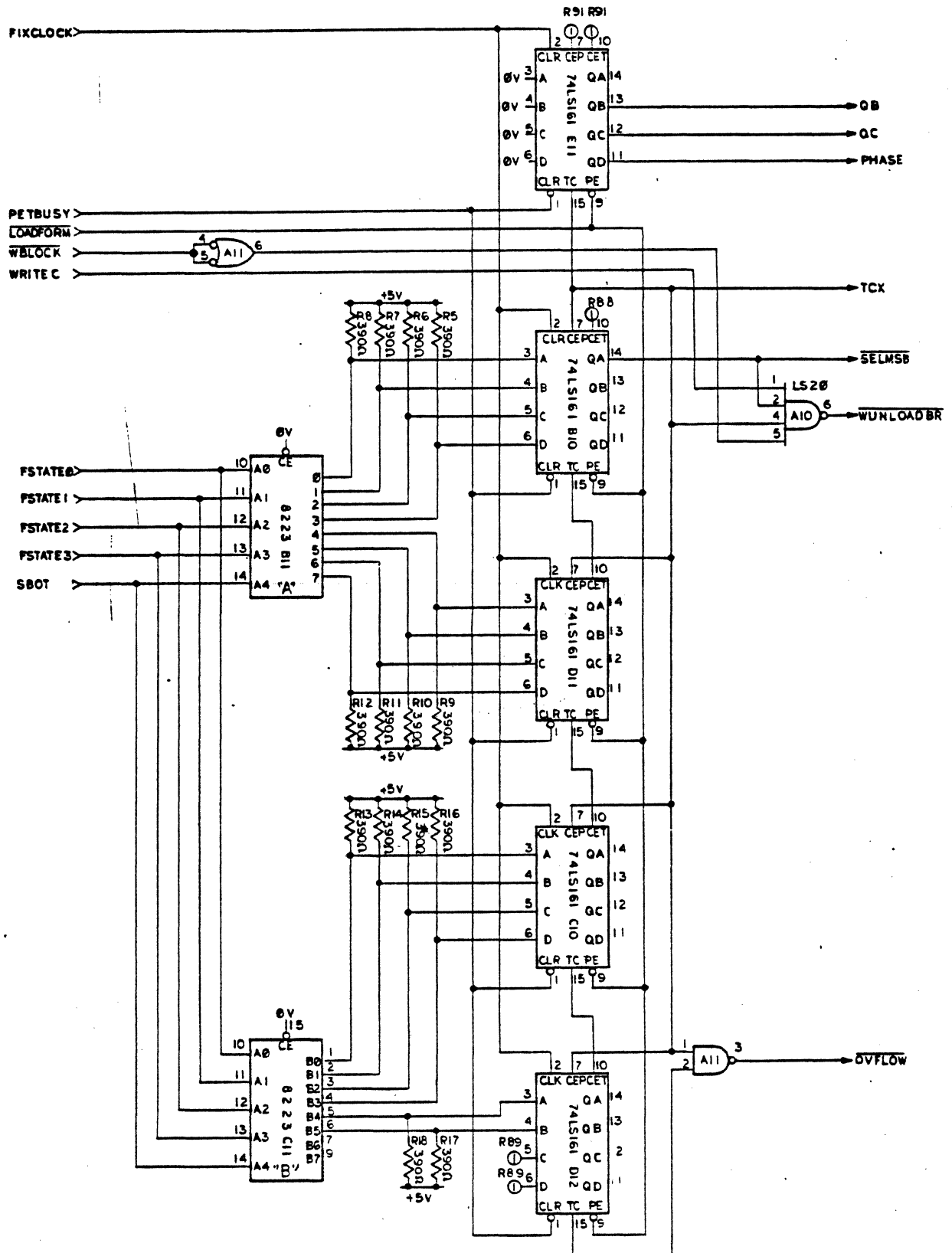


LP3180

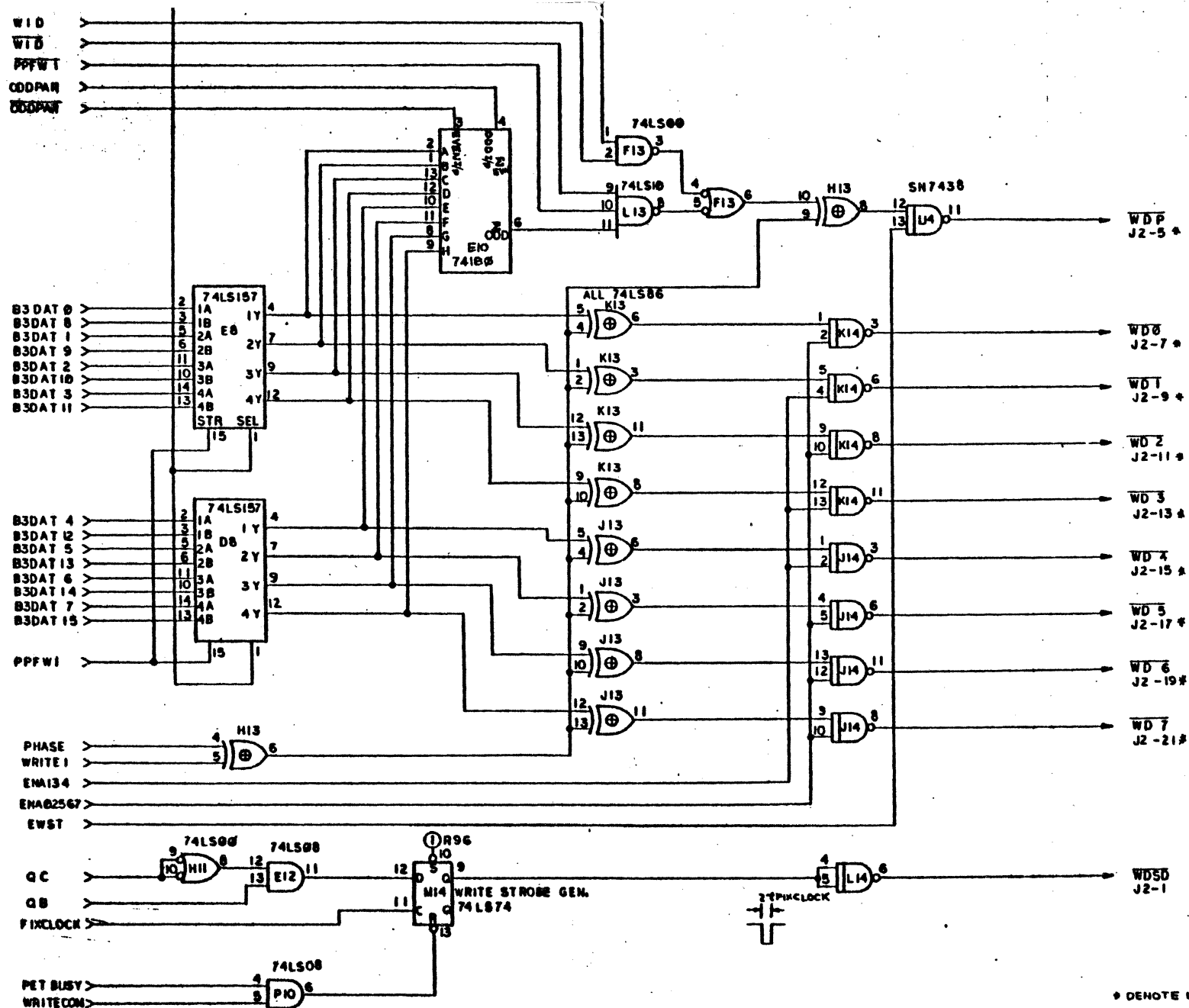
ITEM NO.	REV. NO.	DESCRIPTION	DATE	INITIAL
TOLERANCES				
Count	2	1st PHASE-ENCODER TAP	Done	
APP		2nd PHASE-ENCODER TAP	Done	
APP		3rd PHASE-ENCODER TAP	Done	
APP		4th PHASE-ENCODER TAP	Done	
APP		5th PHASE-ENCODER TAP	Done	
APP		6th PHASE-ENCODER TAP	Done	
APP		7th PHASE-ENCODER TAP	Done	
APP		8th PHASE-ENCODER TAP	Done	
APP		9th PHASE-ENCODER TAP	Done	
APP		10th PHASE-ENCODER TAP	Done	
APP		11th PHASE-ENCODER TAP	Done	
APP		12th PHASE-ENCODER TAP	Done	
APP		13th PHASE-ENCODER TAP	Done	
APP		14th PHASE-ENCODER TAP	Done	
APP		15th PHASE-ENCODER TAP	Done	
APP		16th PHASE-ENCODER TAP	Done	
APP		17th PHASE-ENCODER TAP	Done	
APP		18th PHASE-ENCODER TAP	Done	
APP		19th PHASE-ENCODER TAP	Done	
APP		20th PHASE-ENCODER TAP	Done	
APP		21st PHASE-ENCODER TAP	Done	
APP		22nd PHASE-ENCODER TAP	Done	
APP		23rd PHASE-ENCODER TAP	Done	
APP		24th PHASE-ENCODER TAP	Done	
APP		25th PHASE-ENCODER TAP	Done	
APP		26th PHASE-ENCODER TAP	Done	
APP		27th PHASE-ENCODER TAP	Done	
APP		28th PHASE-ENCODER TAP	Done	
APP		29th PHASE-ENCODER TAP	Done	
APP		30th PHASE-ENCODER TAP	Done	
APP		31st PHASE-ENCODER TAP	Done	
APP		32nd PHASE-ENCODER TAP	Done	
APP		33rd PHASE-ENCODER TAP	Done	
APP		34th PHASE-ENCODER TAP	Done	
APP		35th PHASE-ENCODER TAP	Done	
APP		36th PHASE-ENCODER TAP	Done	
APP		37th PHASE-ENCODER TAP	Done	
APP		38th PHASE-ENCODER TAP	Done	
APP		39th PHASE-ENCODER TAP	Done	
APP		40th PHASE-ENCODER TAP	Done	
APP		41st PHASE-ENCODER TAP	Done	
APP		42nd PHASE-ENCODER TAP	Done	
APP		43rd PHASE-ENCODER TAP	Done	
APP		44th PHASE-ENCODER TAP	Done	
APP		45th PHASE-ENCODER TAP	Done	
APP		46th PHASE-ENCODER TAP	Done	
APP		47th PHASE-ENCODER TAP	Done	
APP		48th PHASE-ENCODER TAP	Done	
APP		49th PHASE-ENCODER TAP	Done	
APP		50th PHASE-ENCODER TAP	Done	
APP		51st PHASE-ENCODER TAP	Done	
APP		52nd PHASE-ENCODER TAP	Done	
APP		53rd PHASE-ENCODER TAP	Done	
APP		54th PHASE-ENCODER TAP	Done	
APP		55th PHASE-ENCODER TAP	Done	
APP		56th PHASE-ENCODER TAP	Done	
APP		57th PHASE-ENCODER TAP	Done	
APP		58th PHASE-ENCODER TAP	Done	
APP		59th PHASE-ENCODER TAP	Done	
APP		60th PHASE-ENCODER TAP	Done	
APP		61st PHASE-ENCODER TAP	Done	
APP		62nd PHASE-ENCODER TAP	Done	
APP		63rd PHASE-ENCODER TAP	Done	
APP		64th PHASE-ENCODER TAP	Done	
APP		65th PHASE-ENCODER TAP	Done	
APP		66th PHASE-ENCODER TAP	Done	
APP		67th PHASE-ENCODER TAP	Done	
APP		68th PHASE-ENCODER TAP	Done	
APP		69th PHASE-ENCODER TAP	Done	
APP		70th PHASE-ENCODER TAP	Done	
APP		71st PHASE-ENCODER TAP	Done	
APP		72nd PHASE-ENCODER TAP	Done	
APP		73rd PHASE-ENCODER TAP	Done	
APP		74th PHASE-ENCODER TAP	Done	
APP		75th PHASE-ENCODER TAP	Done	
APP		76th PHASE-ENCODER TAP	Done	
APP		77th PHASE-ENCODER TAP	Done	
APP		78th PHASE-ENCODER TAP	Done	
APP		79th PHASE-ENCODER TAP	Done	
APP		80th PHASE-ENCODER TAP	Done	
APP		81st PHASE-ENCODER TAP	Done	
APP		82nd PHASE-ENCODER TAP	Done	
APP		83rd PHASE-ENCODER TAP	Done	
APP		84th PHASE-ENCODER TAP	Done	
APP		85th PHASE-ENCODER TAP	Done	
APP		86th PHASE-ENCODER TAP	Done	
APP		87th PHASE-ENCODER TAP	Done	
APP		88th PHASE-ENCODER TAP	Done	
APP		89th PHASE-ENCODER TAP	Done	
APP		90th PHASE-ENCODER TAP	Done	
APP		91st PHASE-ENCODER TAP	Done	
APP		92nd PHASE-ENCODER TAP	Done	
APP		93rd PHASE-ENCODER TAP	Done	
APP		94th PHASE-ENCODER TAP	Done	
APP		95th PHASE-ENCODER TAP	Done	
APP		96th PHASE-ENCODER TAP	Done	
APP		97th PHASE-ENCODER TAP	Done	
APP		98th PHASE-ENCODER TAP	Done	
APP		99th PHASE-ENCODER TAP	Done	
APP		100th PHASE-ENCODER TAP	Done	
APP		101st PHASE-ENCODER TAP	Done	
APP		102nd PHASE-ENCODER TAP	Done	
APP		103rd PHASE-ENCODER TAP	Done	
APP		104th PHASE-ENCODER TAP	Done	
APP		105th PHASE-ENCODER TAP	Done	
APP		106th PHASE-ENCODER TAP	Done	
APP		107th PHASE-ENCODER TAP	Done	
APP		108th PHASE-ENCODER TAP	Done	
APP		109th PHASE-ENCODER TAP	Done	
APP		110th PHASE-ENCODER TAP	Done	
APP		111th PHASE-ENCODER TAP	Done	
APP		112th PHASE-ENCODER TAP	Done	
APP		113th PHASE-ENCODER TAP	Done	
APP		114th PHASE-ENCODER TAP	Done	
APP		115th PHASE-ENCODER TAP	Done	
APP		116th PHASE-ENCODER TAP	Done	
APP		117th PHASE-ENCODER TAP	Done	
APP		118th PHASE-ENCODER TAP	Done	
APP		119th PHASE-ENCODER TAP	Done	
APP		120th PHASE-ENCODER TAP	Done	
APP		121st PHASE-ENCODER TAP	Done	
APP		122nd PHASE-ENCODER TAP	Done	
APP		123rd PHASE-ENCODER TAP	Done	
APP		124th PHASE-ENCODER TAP	Done	
APP		125th PHASE-ENCODER TAP	Done	
APP		126th PHASE-ENCODER TAP	Done	
APP		127th PHASE-ENCODER TAP	Done	
APP		128th PHASE-ENCODER TAP	Done	
APP		129th PHASE-ENCODER TAP	Done	
APP		130th PHASE-ENCODER TAP	Done	
APP		131st PHASE-ENCODER TAP	Done	
APP		132nd PHASE-ENCODER TAP	Done	
APP		133rd PHASE-ENCODER TAP	Done	
APP		134th PHASE-ENCODER TAP	Done	
APP		135th PHASE-ENCODER TAP	Done	
APP		136th PHASE-ENCODER TAP	Done	
APP		137th PHASE-ENCODER TAP	Done	
APP		138th PHASE-ENCODER TAP	Done	
APP		139th PHASE-ENCODER TAP	Done	
APP		140th PHASE-ENCODER TAP	Done	
APP		141st PHASE-ENCODER TAP	Done	
APP		142nd PHASE-ENCODER TAP	Done	
APP		143rd PHASE-ENCODER TAP	Done	
APP		144th PHASE-ENCODER TAP	Done	
APP		145th PHASE-ENCODER TAP	Done	
APP		146th PHASE-ENCODER TAP	Done	
APP		147th PHASE-ENCODER TAP	Done	
APP		148th PHASE-ENCODER TAP	Done	
APP		149th PHASE-ENCODER TAP	Done	
APP		150th PHASE-ENCODER TAP	Done	
APP		151st PHASE-ENCODER TAP	Done	
APP		152nd PHASE-ENCODER TAP	Done	
APP		153rd PHASE-ENCODER TAP	Done	
APP		154th PHASE-ENCODER TAP	Done	
APP		155th PHASE-ENCODER TAP	Done	
APP		156th PHASE-ENCODER TAP	Done	
APP		157th PHASE-ENCODER TAP	Done	
APP		158th PHASE-ENCODER TAP	Done	
APP		159th PHASE-ENCODER TAP	Done	
APP		160th PHASE-ENCODER TAP	Done	
APP		161st PHASE-ENCODER TAP	Done	
APP		162nd PHASE-ENCODER TAP	Done	
APP		163rd PHASE-ENCODER TAP	Done	
APP		164th PHASE-ENCODER TAP	Done	
APP		165th PHASE-ENCODER TAP	Done	
APP		166th PHASE-ENCODER TAP	Done	
APP		167th PHASE-ENCODER TAP	Done	
APP		168th PHASE-ENCODER TAP	Done	
APP		169th PHASE-ENCODER TAP	Done	
APP		170th PHASE-ENCODER TAP	Done	
APP		171st PHASE-ENCODER TAP	Done	
APP		172nd PHASE-ENCODER TAP	Done	
APP		173rd PHASE-ENCODER TAP	Done	
APP		174th PHASE-ENCODER TAP	Done	
APP		175th PHASE-ENCODER TAP	Done	
APP		176th PHASE-ENCODER TAP	Done	
APP		177th PHASE-ENCODER TAP	Done	
APP		178th PHASE-ENCODER TAP	Done	
APP		179th PHASE-ENCODER TAP	Done	
APP		180th PHASE-ENCODER TAP	Done	
APP		181st PHASE-ENCODER TAP	Done	
APP		182nd PHASE-ENCODER TAP	Done	
APP		183rd PHASE-ENCODER TAP	Done	
APP		184th PHASE-ENCODER TAP	Done	
APP		185th PHASE-ENCODER TAP	Done	
APP		186th PHASE-ENCODER TAP	Done	
APP		187th PHASE-ENCODER TAP	Done	
APP		188th PHASE-ENCODER TAP	Done	
APP		189th PHASE-ENCODER TAP	Done	
APP		190th PHASE-ENCODER TAP	Done	
APP		191st PHASE-ENCODER TAP	Done	
APP		192nd PHASE-ENCODER TAP	Done	
APP		193rd PHASE-ENCODER TAP	Done	
APP		194th PHASE-ENCODER TAP	Done	
APP		195th PHASE-ENCODER TAP	Done	
APP		196th PHASE-ENCODER TAP	Done	
APP		197th PHASE-ENCODER TAP	Done	
APP		198th PHASE-ENCODER TAP	Done	
APP		199th PHASE-ENCODER TAP	Done	
APP		200th PHASE-ENCODER TAP	Done	
APP		201st PHASE-ENCODER TAP	Done	
APP		202nd PHASE-ENCODER TAP	Done	
APP		203rd PHASE-ENCODER TAP	Done	
APP		204th PHASE-ENCODER TAP	Done	
APP		205th PHASE-ENCODER TAP	Done	
APP		206th PHASE-ENCODER TAP	Done	
APP		207th PHASE-ENCODER TAP	Done	
APP		208th PHASE-ENCODER TAP	Done	
APP		209th PHASE-ENCODER TAP	Done	
APP		210th PHASE-ENCODER TAP	Done	
APP		211st PHASE-ENCODER TAP	Done	
APP		212nd PHASE-ENCODER TAP	Done	
APP		213rd PHASE-ENCODER TAP	Done	
APP		214th PHASE-ENCODER TAP	Done	
APP		215th PHASE-ENCODER TAP	Done	
APP		216th PHASE-ENCODER TAP	Done	
APP		217th PHASE-ENCODER TAP	Done	
APP		218th PHASE-ENCODER TAP	Done	
APP		219th PHASE-ENCODER TAP	Done	
APP		220th PHASE-ENCODER TAP	Done	
APP		221st PHASE-ENCODER TAP	Done	
APP		222nd PHASE-ENCODER TAP	Done	
APP		223rd PHASE-ENCODER TAP	Done	
APP		224th PHASE-ENCODER TAP	Done	
APP		225th PHASE-ENCODER TAP	Done	
APP		226th PHASE-ENCODER TAP	Done	
APP		227th PHASE-ENCODER TAP	Done	
APP		228th PHASE-ENCODER TAP	Done	
APP		229th PHASE-ENCODER TAP	Done	
APP		230th PHASE-ENCODER TAP	Done	
APP		231st PHASE-ENCODER TAP	Done	
APP		232nd PHASE-ENCODER TAP	Done	
APP		233rd PHASE-ENCODER TAP	Done	
APP		234th PHASE-ENCOD		







STATE DURATION COUNTER



→ DENOTE LINE TO TAPE UNIT

TAPE PHASE ENCODERS, WRITE
VERTICAL PARITY

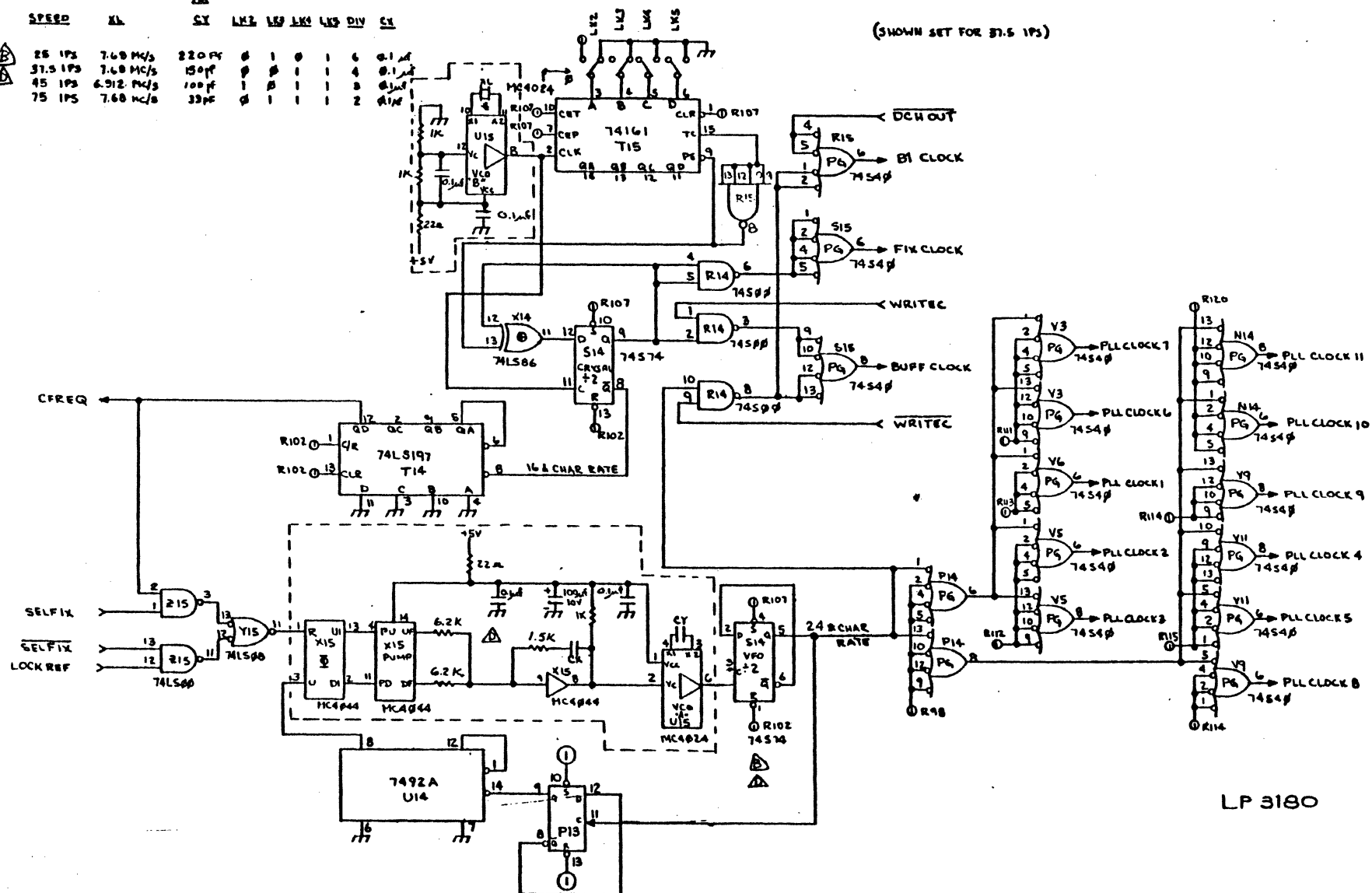
96-0203474-7 F 6 32

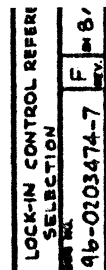
TAPE PHASE ENCODERS, WR
VERTICAL PARITY
96-0203474-7 F 6 32

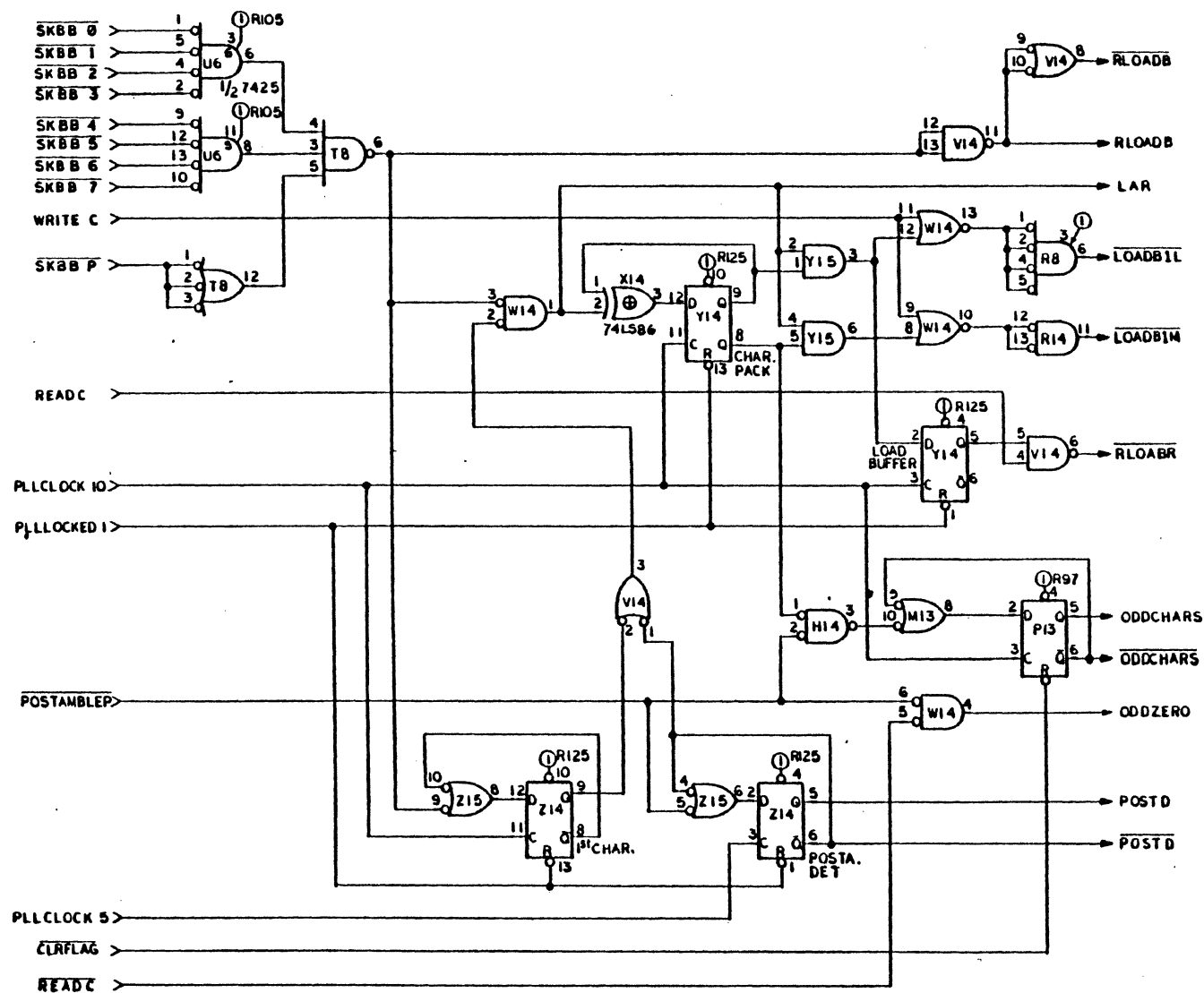
SPEED XL CY LK2 LK3 LK4 LK5 DIV CY

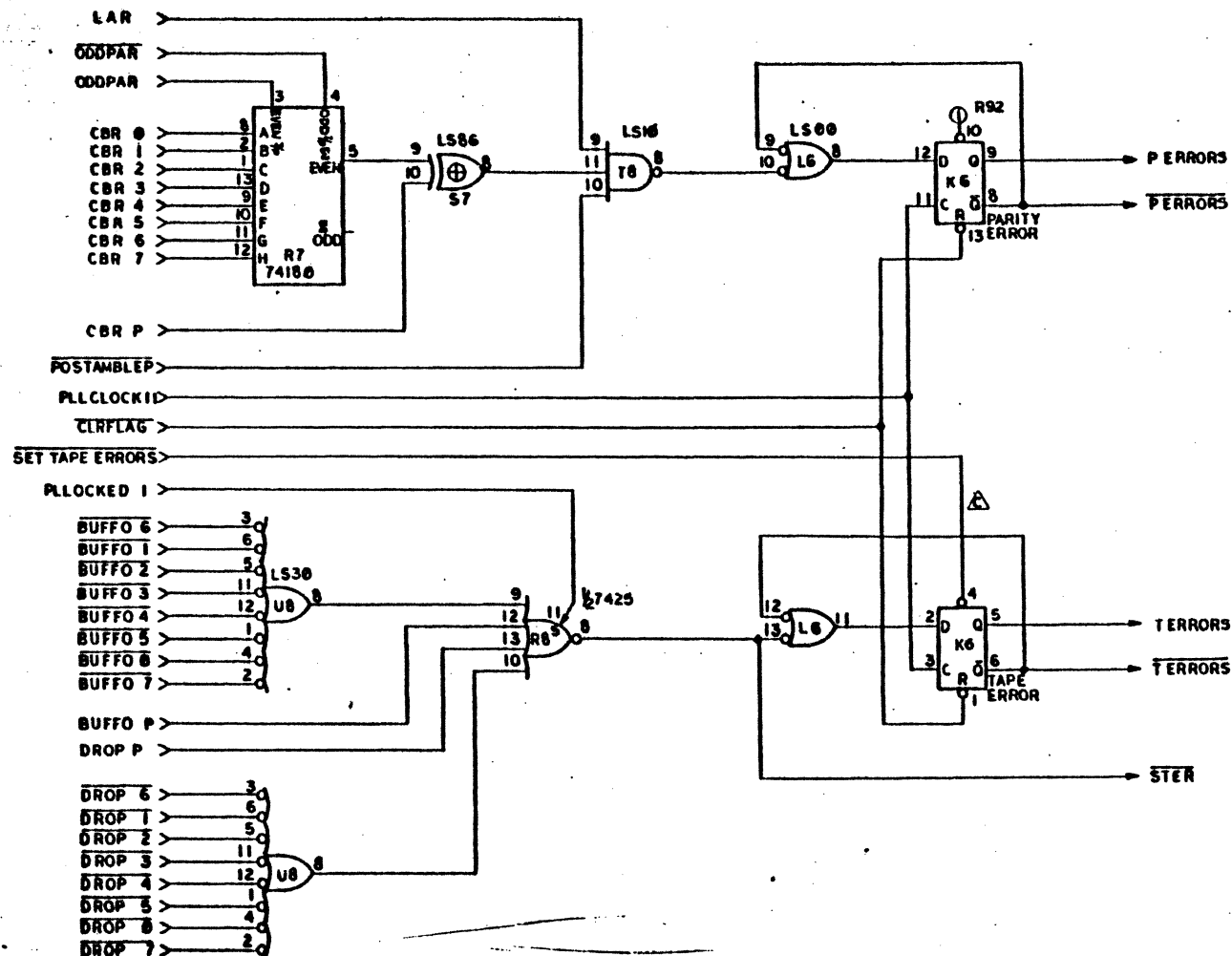
25 IPS	7.68 MC/s	220 pF	0	1	0	1	6	0.1 μ F
37.5 IPS	7.68 MC/s	150 pF	0	0	1	1	4	0.1 μ F
45 IPS	6.912 MC/s	100 pF	1	0	1	1	3	0.1 μ F
75 IPS	7.68 MC/s	33 pF	0	1	1	1	2	0.1 μ F

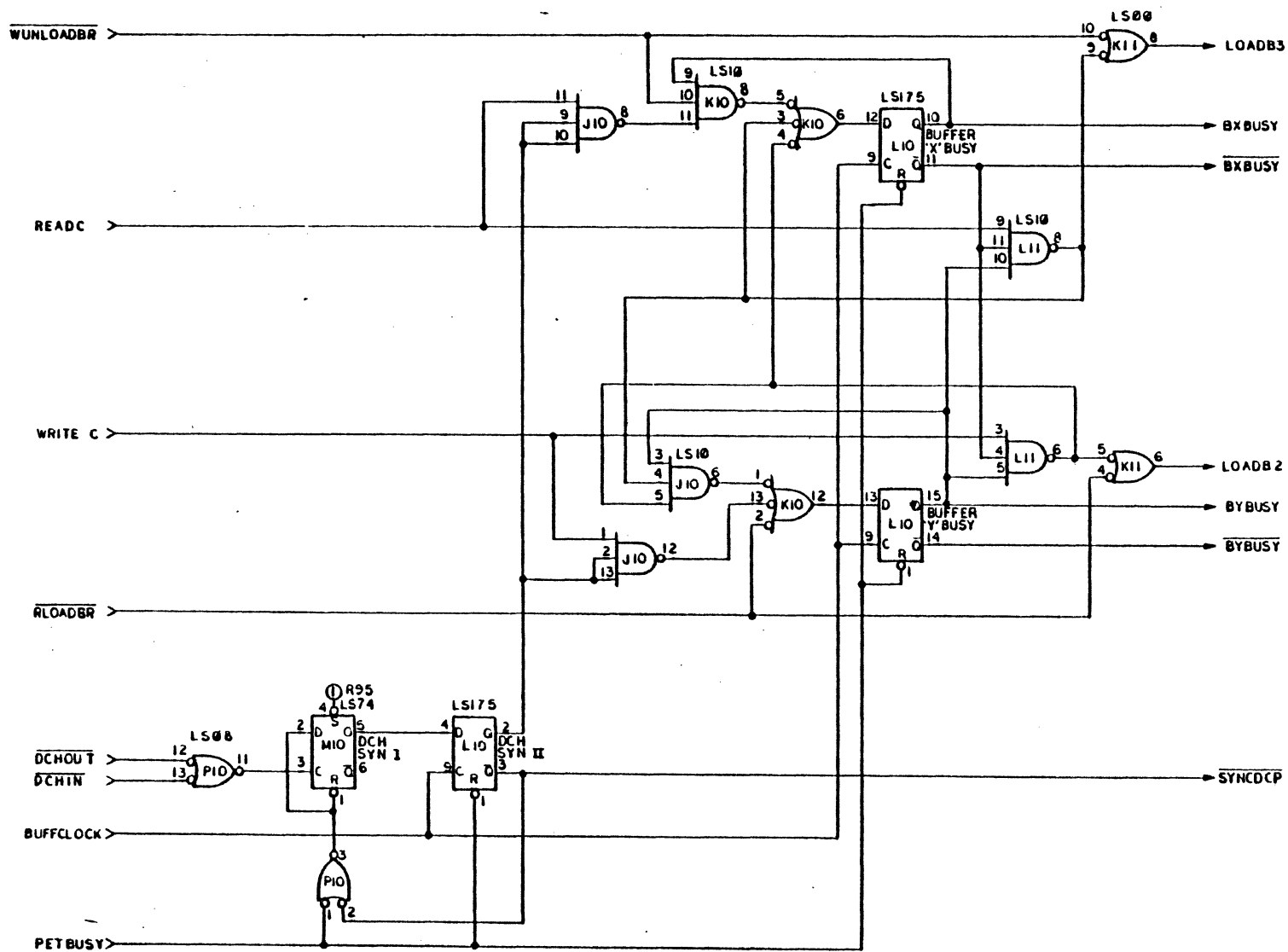
(SHOWN SET FOR 37.5 IPS)











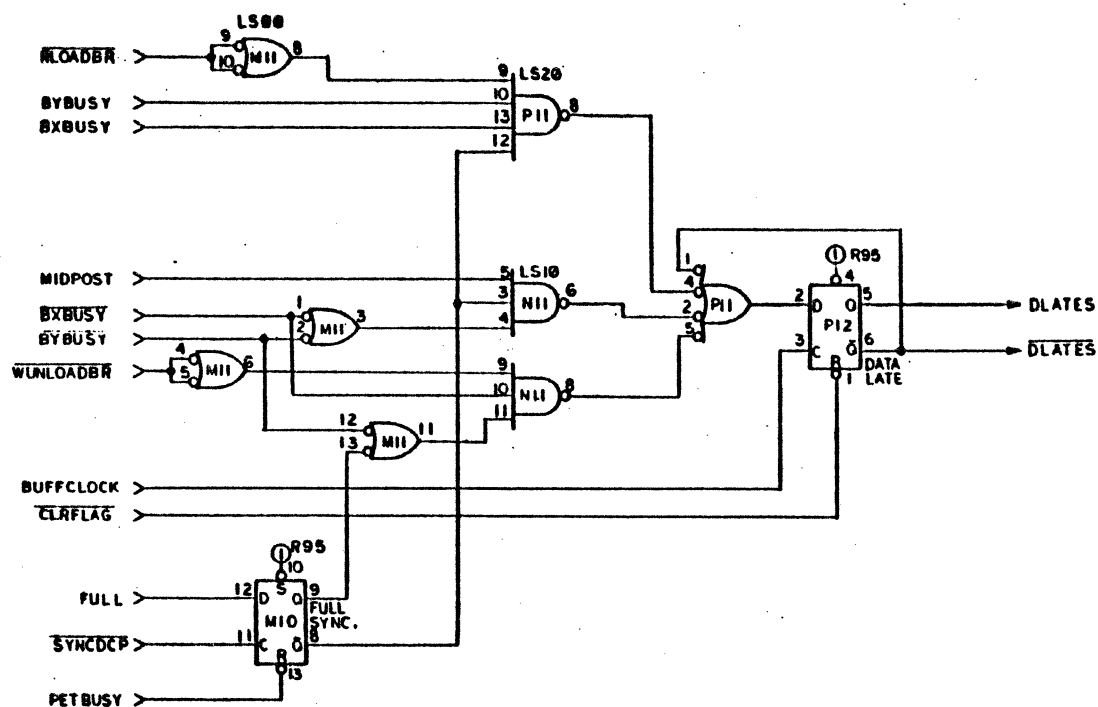
BUFFER CONTROL

96-0203474-7

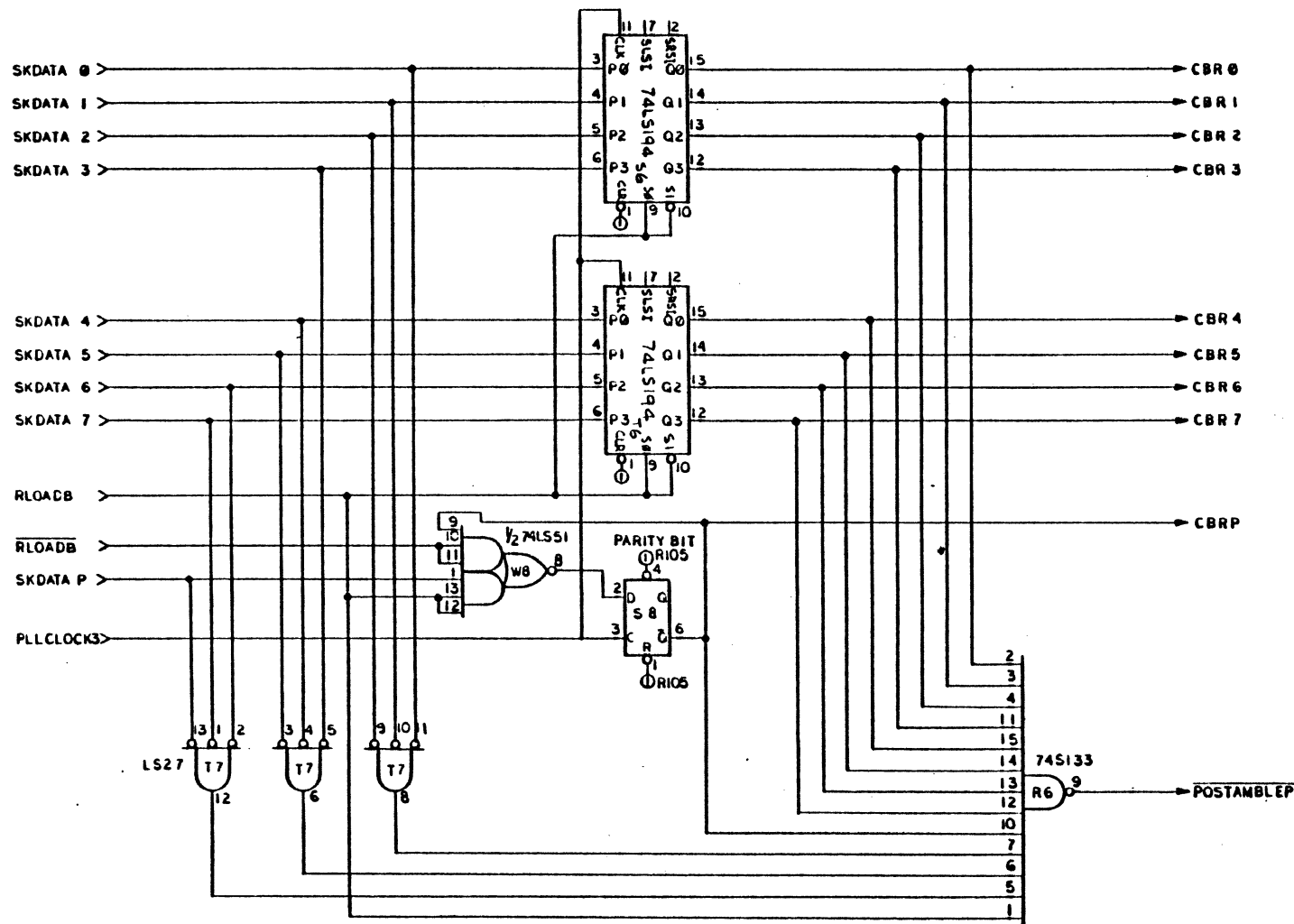
F

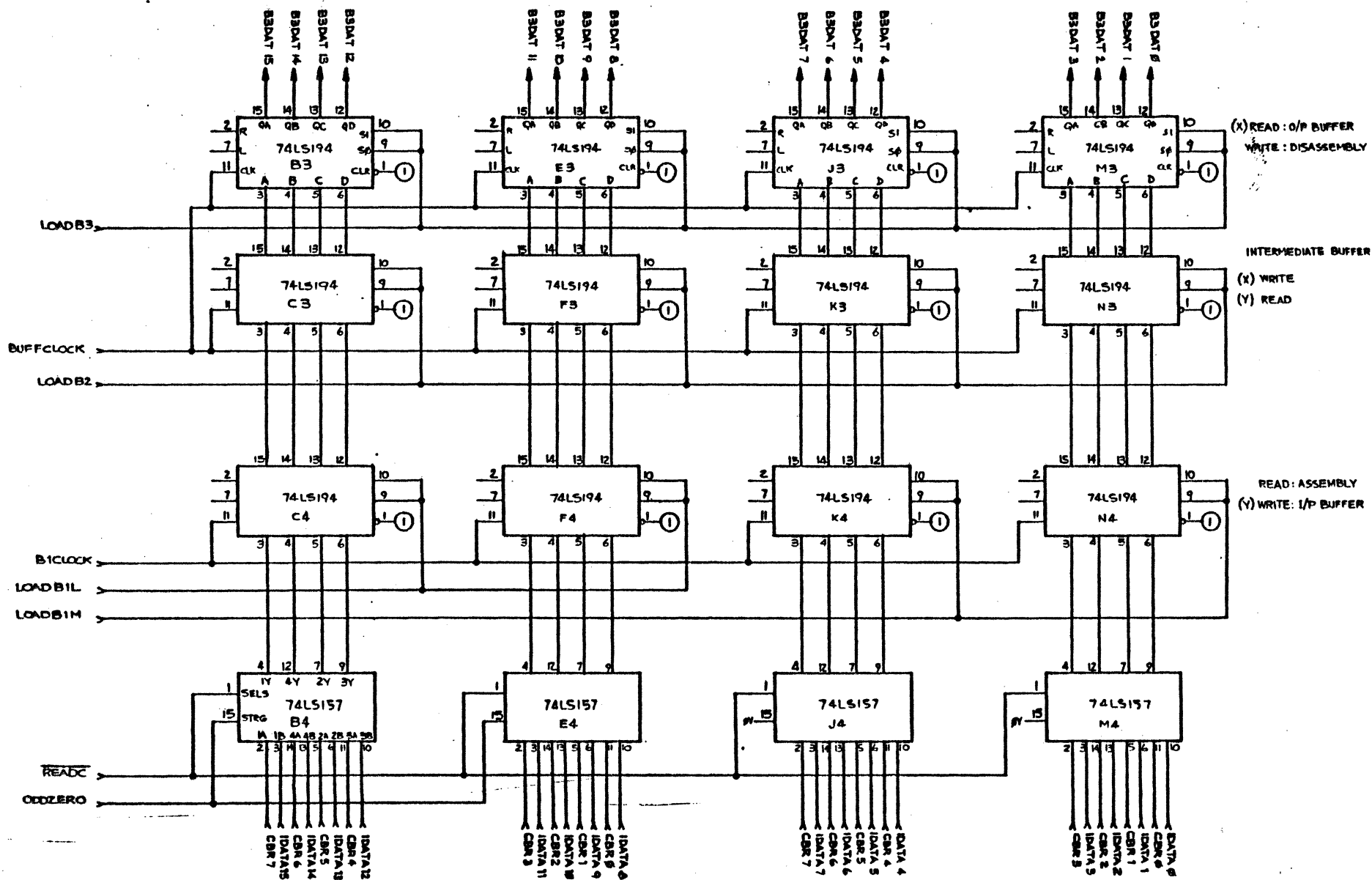
11/32

BUFFER CONTROL



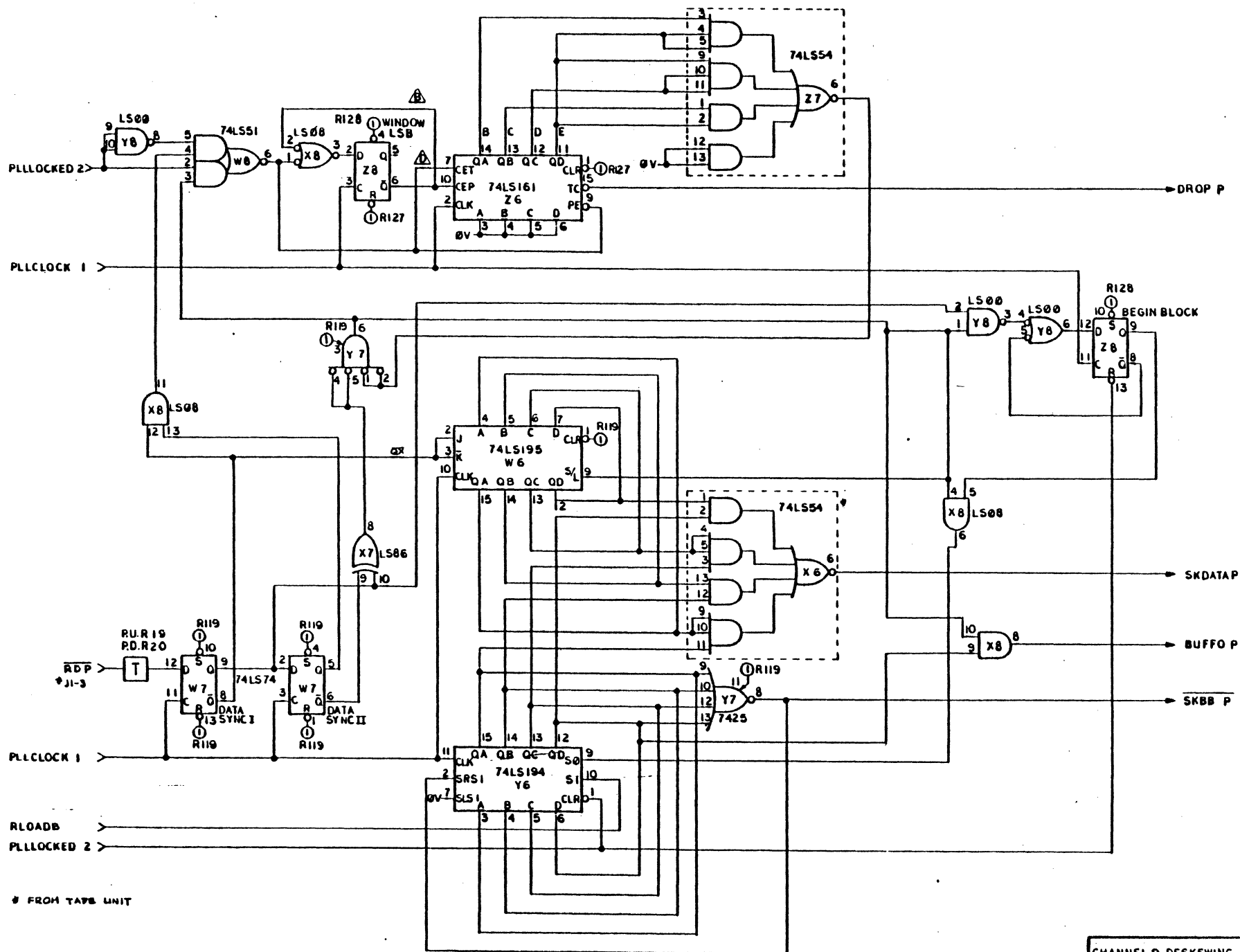
NOTE: THE CIRCUIT PRESENTED HEREON WILL DETECT ALL 'DATA LATE' ERRORS, HOWEVER IT WILL RESPOND ALSO TO SLUGGISH DATA-CHANNEL ACTION FOR SEVERAL WORDS DURING READ AFTER BLOCK TRANSFER, THIS CIRCUIT HAS BEEN USED IN ORDER TO CONSERVE CIRCUIT BOARD SPACE.

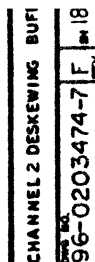


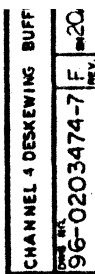


CHANNEL BUFFERS

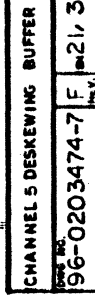
Doc No
96-0203474-7 F SH 14/32

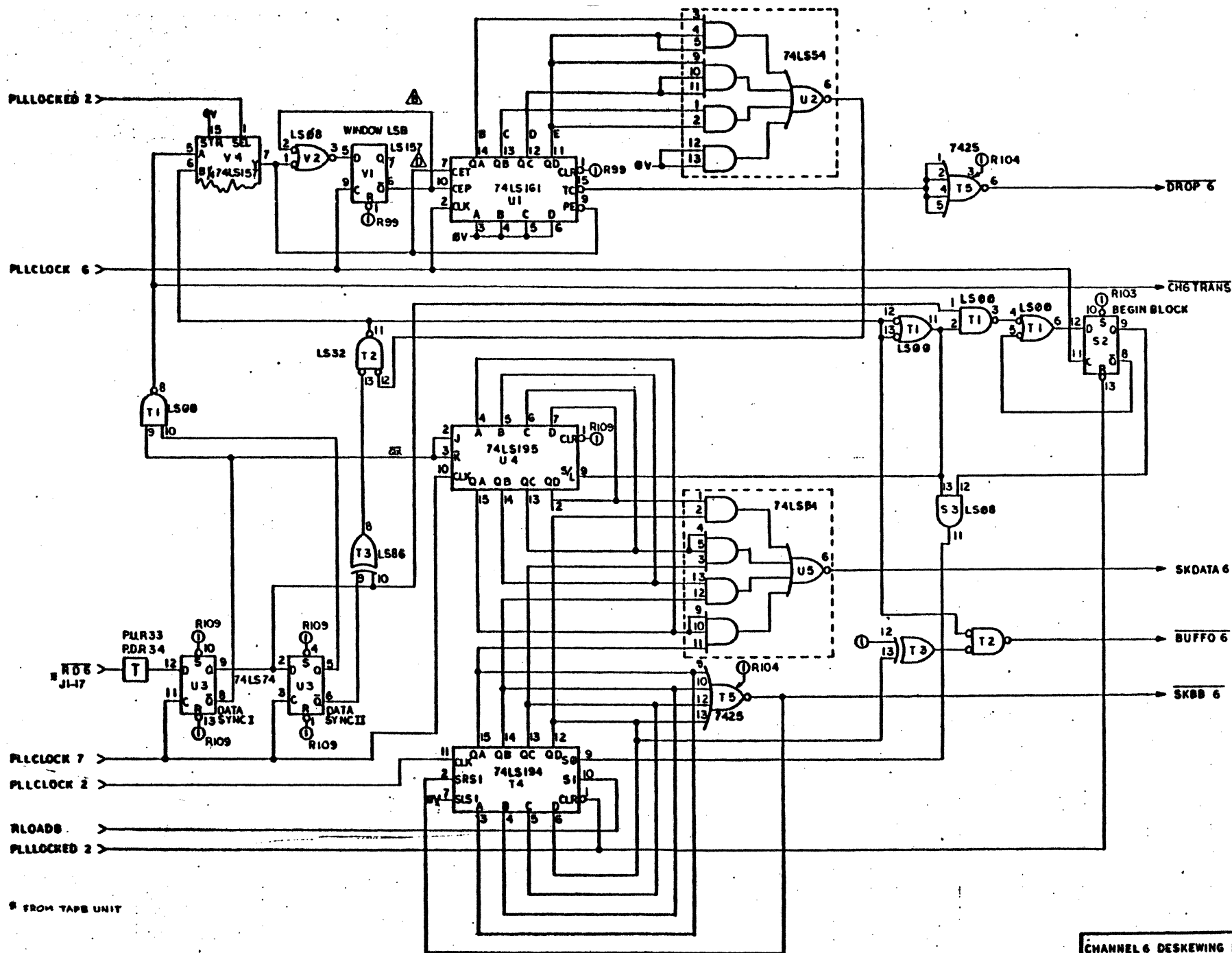




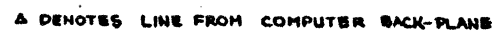


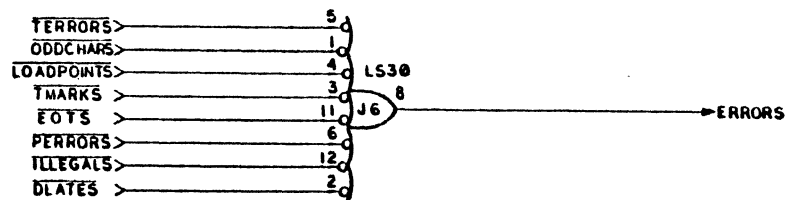
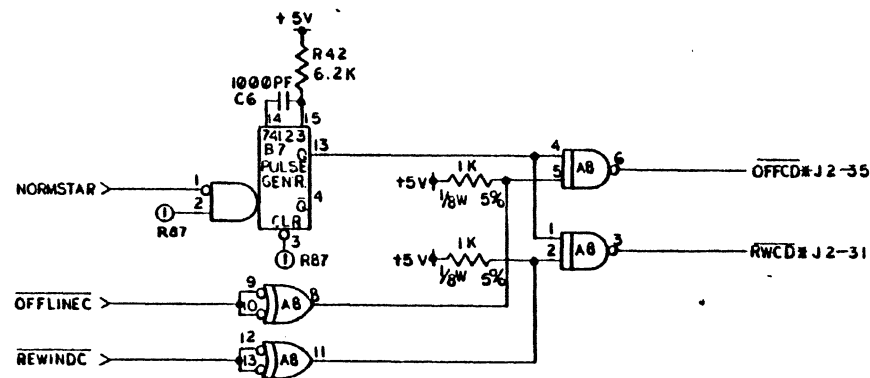
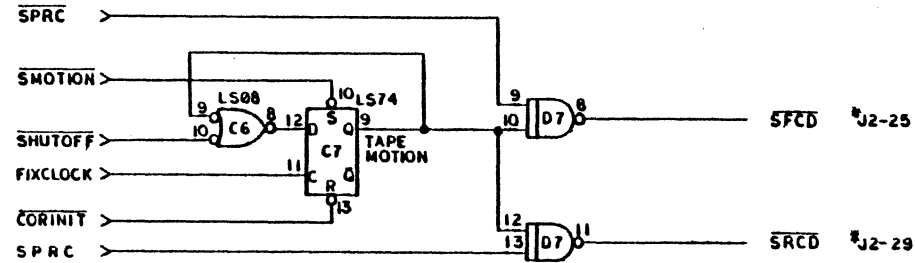
96-0203474-7 F SH 20 32



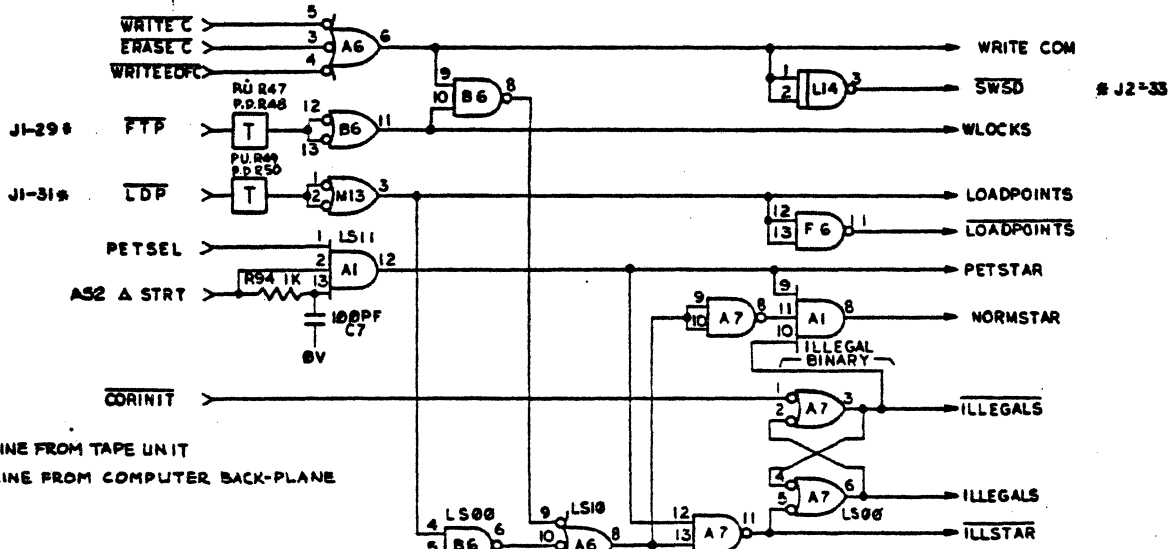
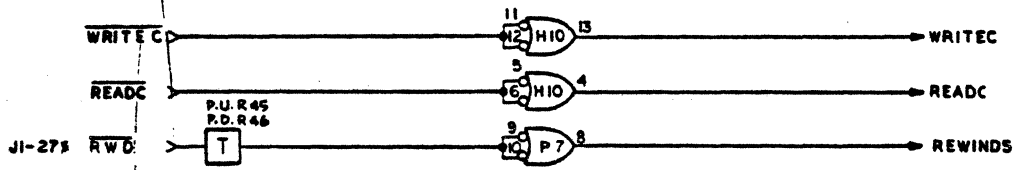
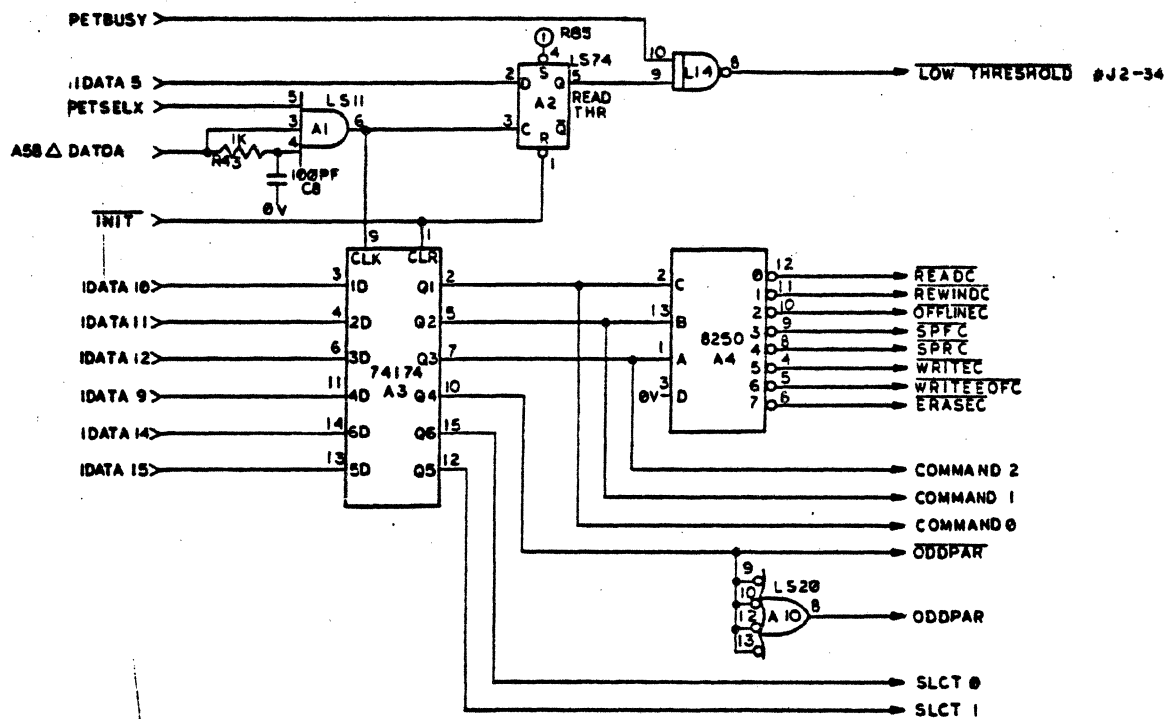






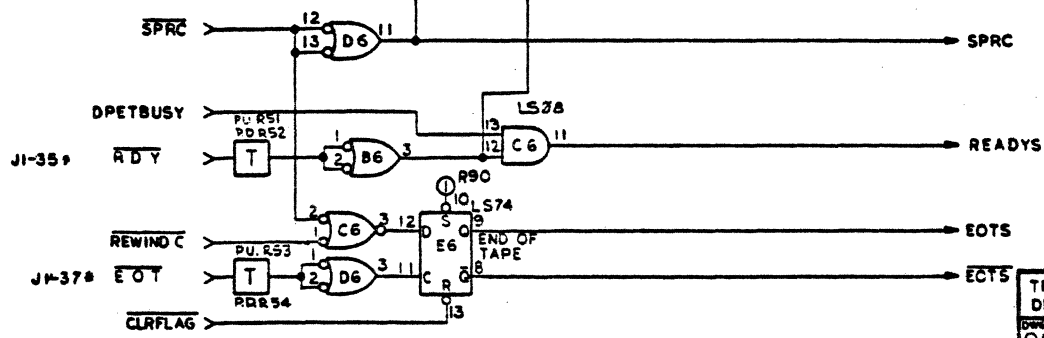


* DENOTES LINE FROM TAPE UNIT

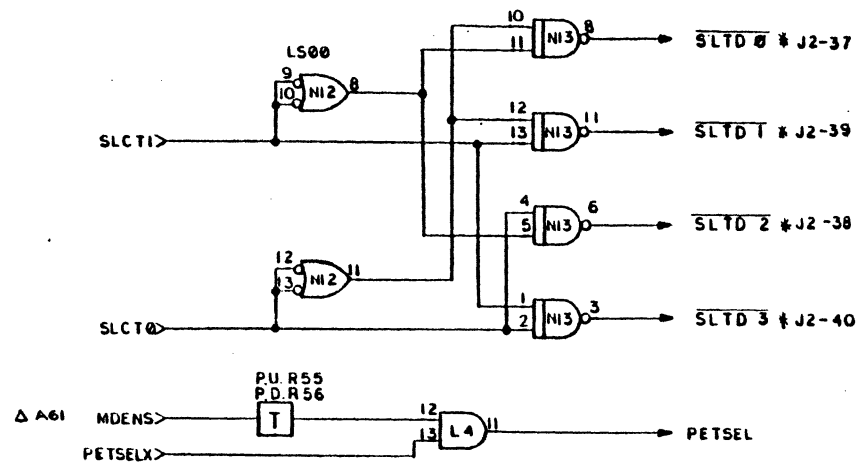


* DENOTES LINE FROM TAPE UNIT
 Δ DENOTES LINE FROM COMPUTER BACK-PLANE

TRANSPORT STATUS COMMAND
 DECODER
 96-0203474-7 F
 REV. 26/32



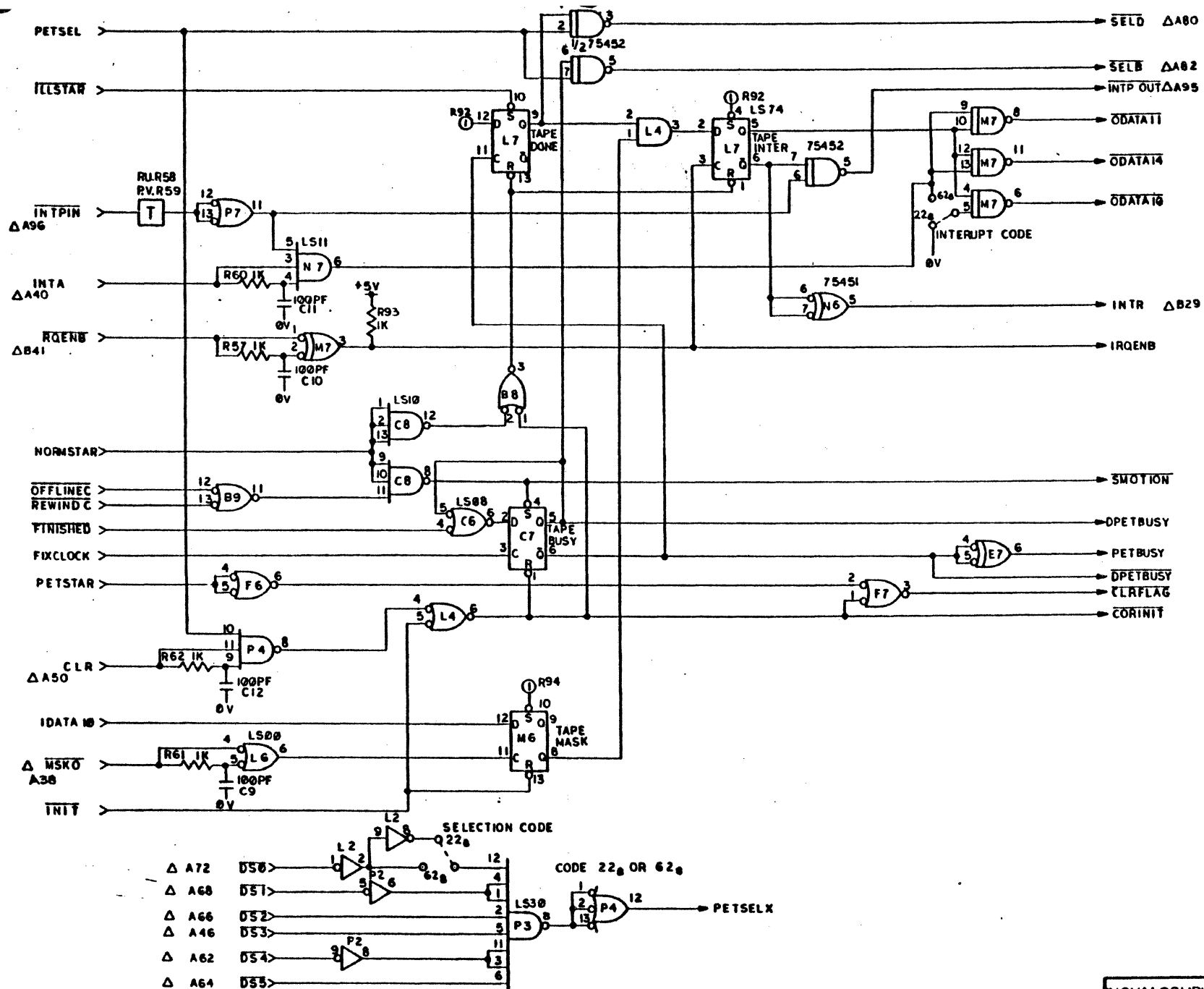
TRANSPORT STATUS COMMAND
 DECODER
 96-0203474-7 F
 REV. 26/32



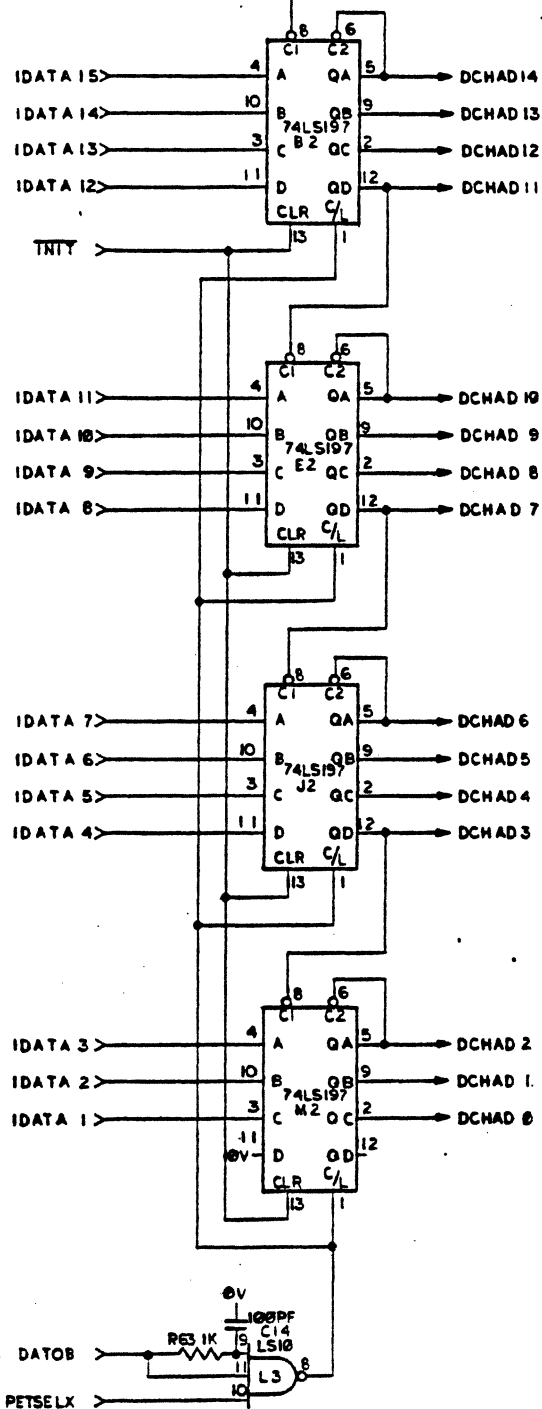
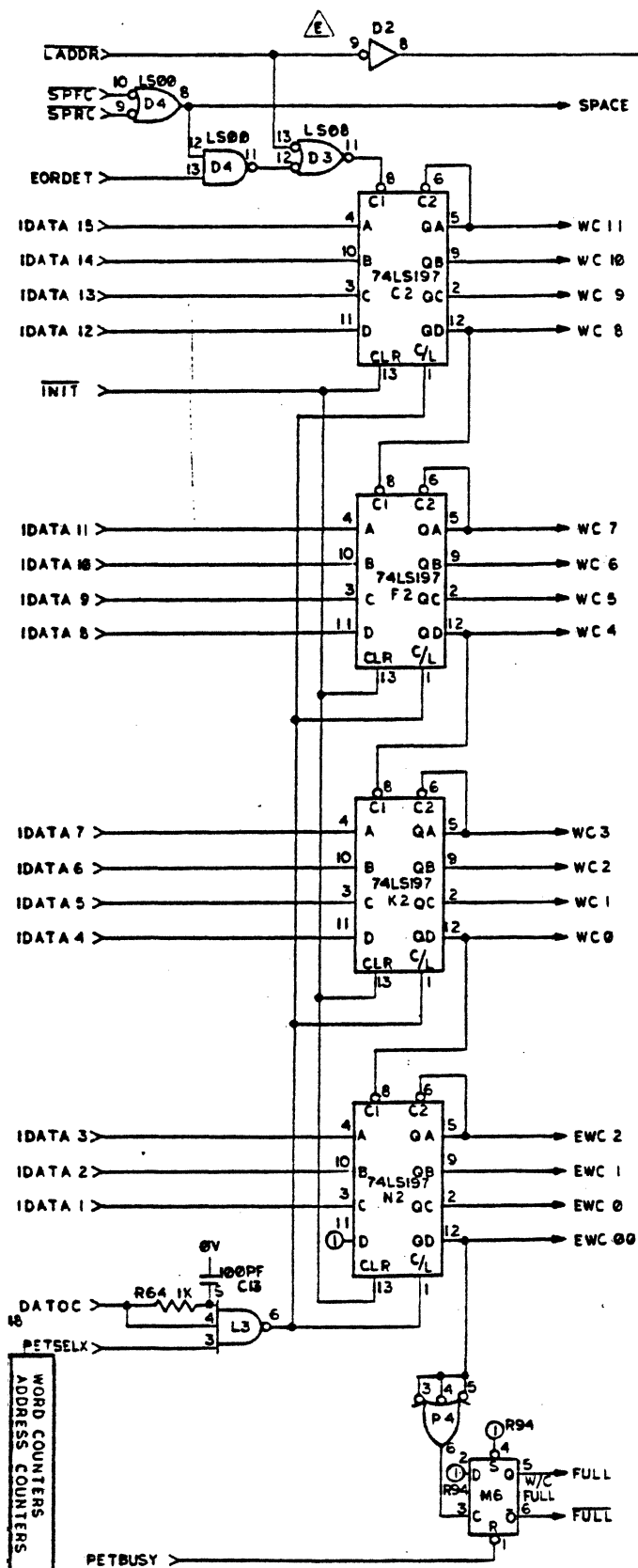
NOTE FOR MULTI-DENSITY WORKING

- 1) 3120 HOLDS MDENS HIGH FOR PHASE-ENCODED OPERATION. (3180/20 OPTION)
- 2) THE PROGRAM MUST ENSURE THAT THE DRIVE BEING ADDRESSED IS HELD IN A FIXED MODE FOR THE DURATION OF ALL COMMANDS EXECUTED UPON IT.
- 3) AS THE INTERFACE SELECTED IS A FUNCTION OF THE DENSITY OF THE TAPE, ALL OPERATIONS UPON A GIVEN INTERFACE SHOULD BE CONCLUDED PRIOR TO SELECTION OF ANOTHER TAPE UNIT.

Δ DENOTES LINE FROM COMPUTER BACK-PLANE



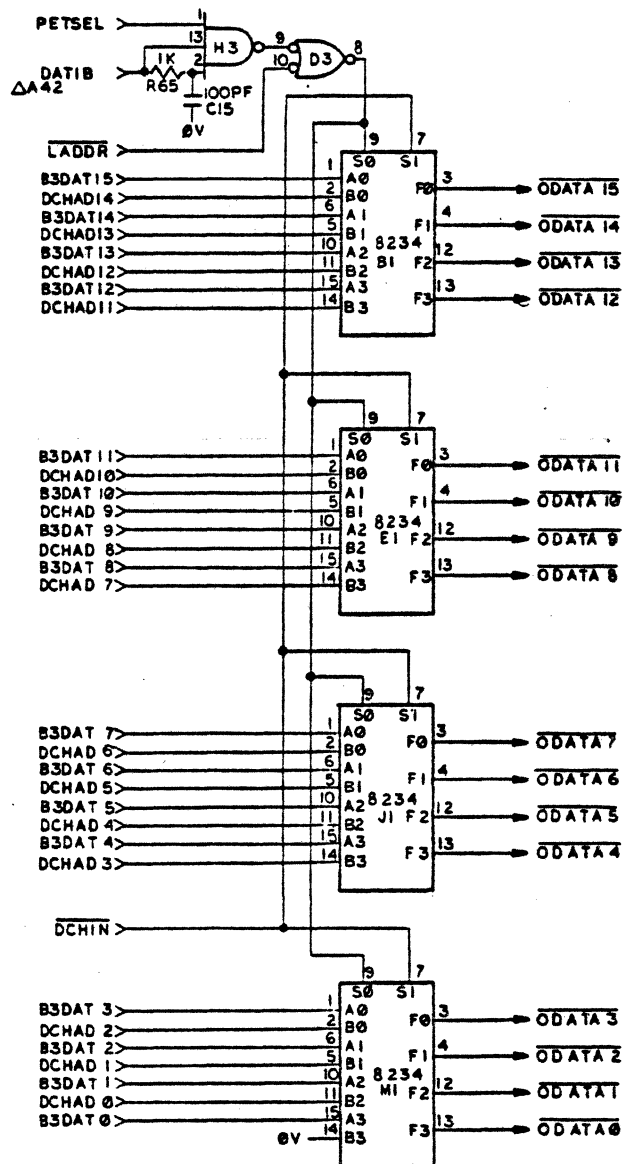
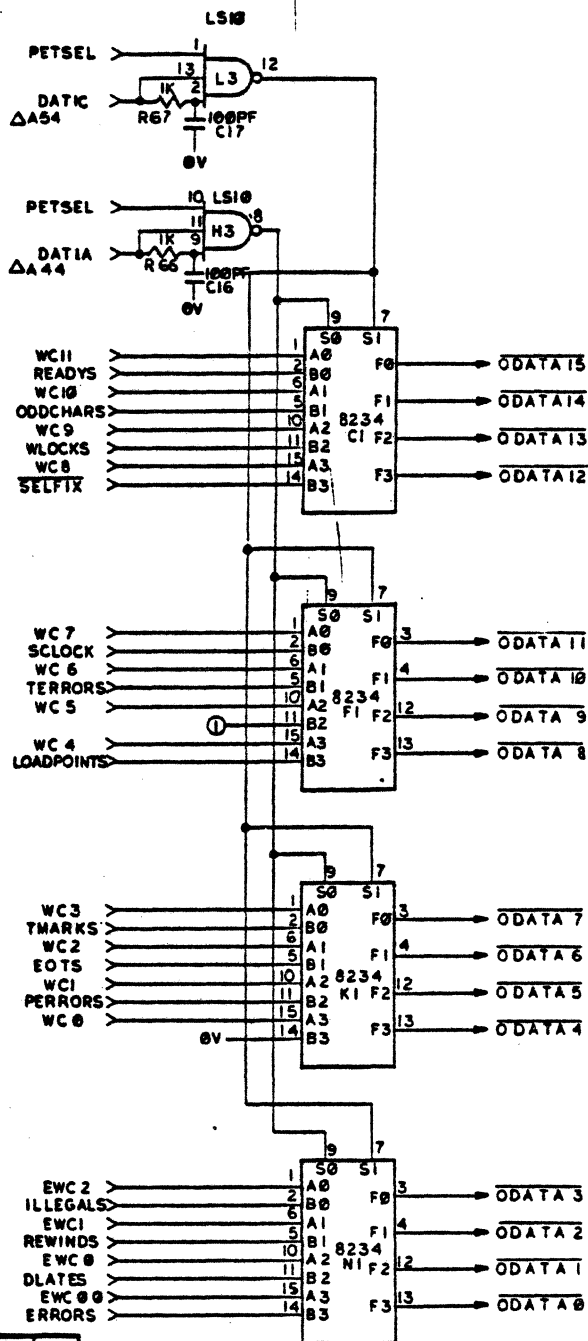
Δ DENOTES LINE FROM COMPUTER BACK-PLANE



Δ DENOTES LINE FROM COMPUTER BACK-PLANE

WORD COUNTERS
ADDRESS COUNTERS

96-02 03474-7 F REV. 29/32



DATA OUTPUT SWITCH STATUS

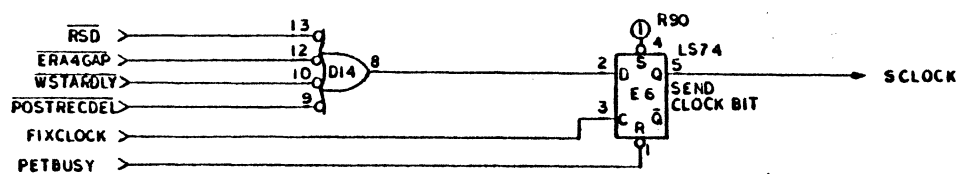
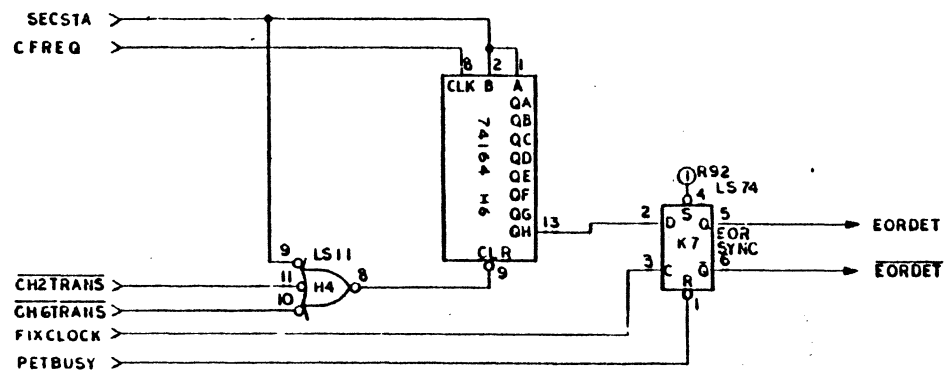
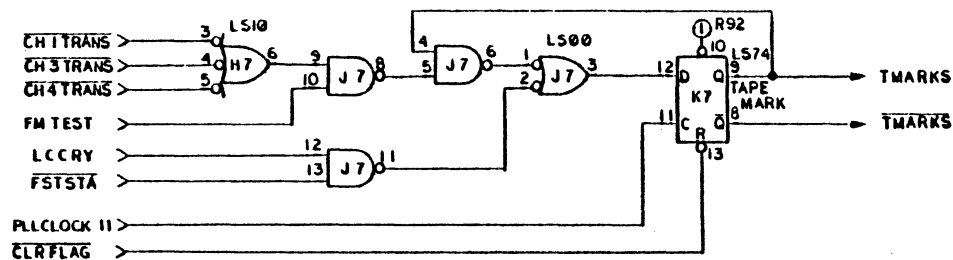
96-0203474-7

REV. 30/32

DATA OUTPUT SWITCH STATUS

96-0203474-7

REV. 30/32

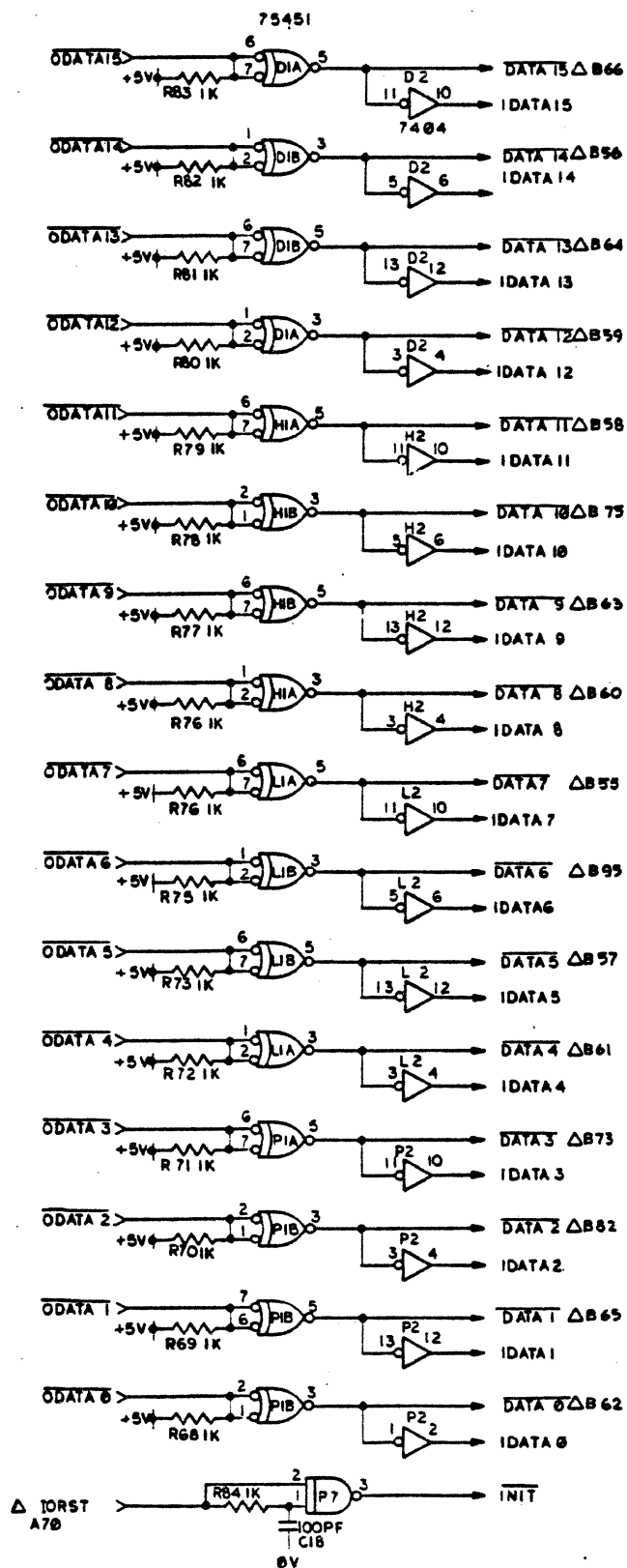


TAPE MARK DETECTOR
BLOCK GAP DETECTORS

Rev. No. 96-0203474-7

3/32

TAPE-MARK DETECTOR
BLOCK-GAP DETECTORS



Δ DENOTES LINE FROM COMPUTER BACK PANEL

is hereby and shall not be disclosed, used or duplicated in whole or in part, for any purpose whatsoever without prior written permission of Ball Computer Products, 8801 College Avenue, Oakland, California 94618. This legend shall be marked on any reproduction hereof in whole or in part. Receipt of this document shall be deemed to be an acceptance of the conditions specified herein.

LTR	DESCRIPTION	DATE	APP
A	DOCUMENTATION RELEASE E.O. 12553	2/11/75	<i>ELL</i>
B	REF E.O. 1488	10-18-75	<i>DEL</i>

SHEET TITLE

2. I/O ADAPTER - CONTROLLER INPUT
3. I/O ADAPTER - CONTROLLER OUTPUT

96-0204252-5 B

91-0202352-0		UNIT 3120 and 3180		 Ball Computer Products, Inc. OAKLAND, CA 94618	
DRAWN LINDSTEDT		DATE 2/75		SCHEMATIC I/O ADAPTER	
CHECK S. SMITH		2/75			
DESIGN					
APP BY <i>ELL</i>		2/75			
		SIZE C	DWS. NO. 96-0204252-5		B REV

